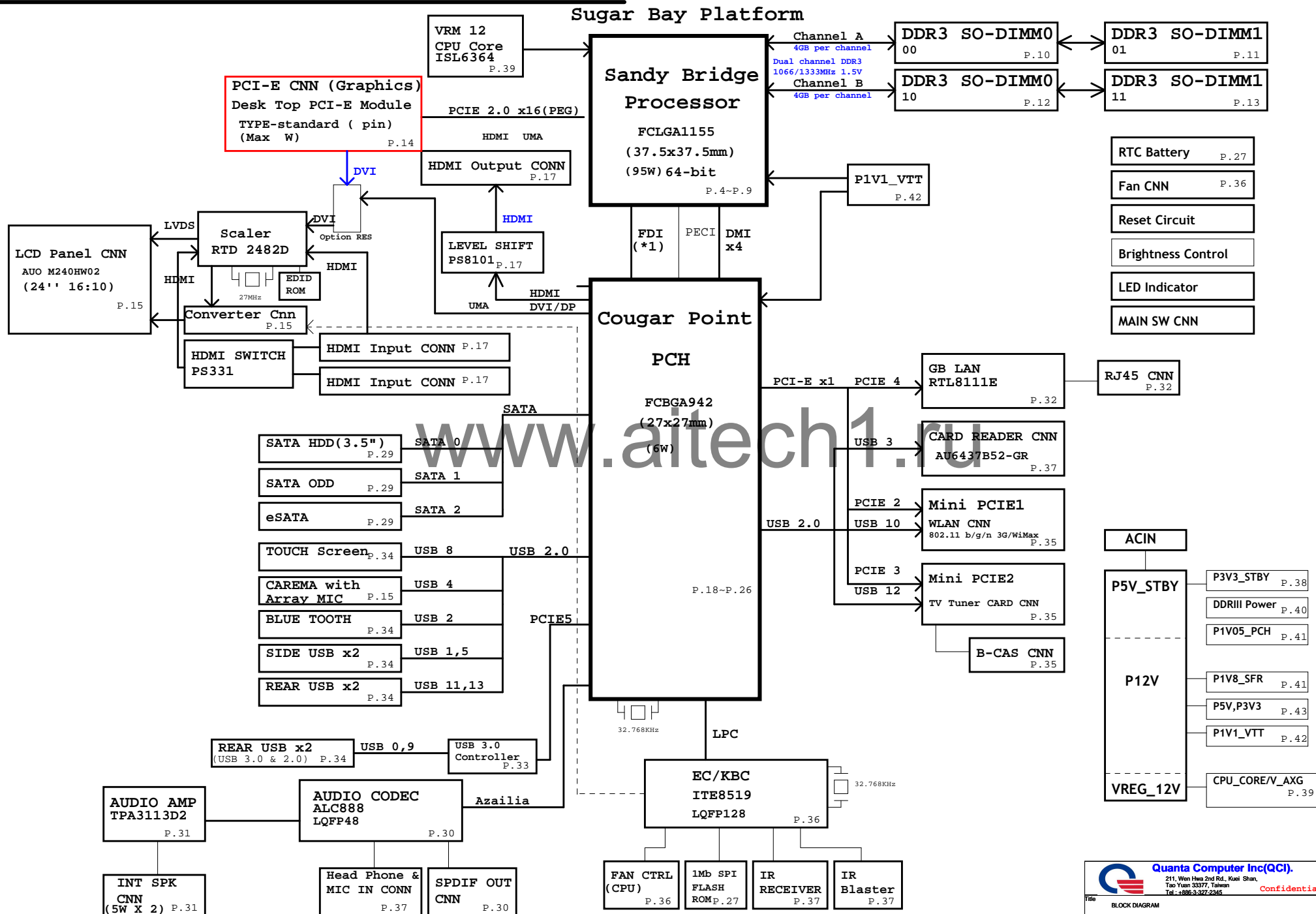


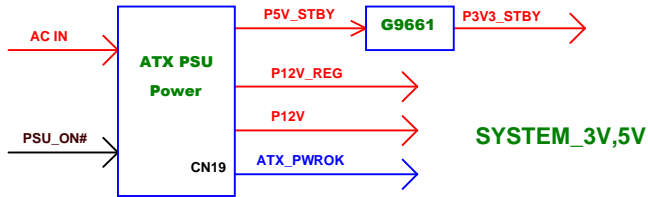
# QK1 24" AIO Block Diagram :

1

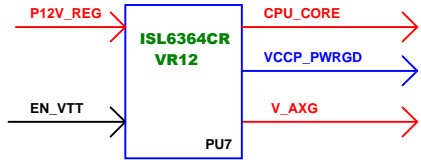


## Power rail control

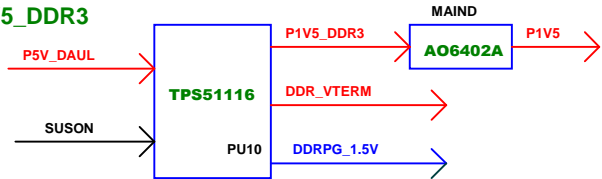
## PSU



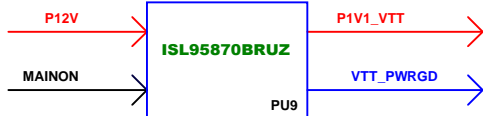
## CPU\_CORE/V\_AXG



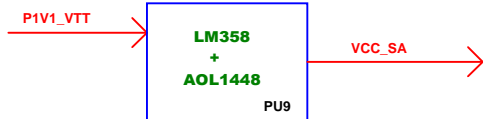
## P1V5\_DDR3



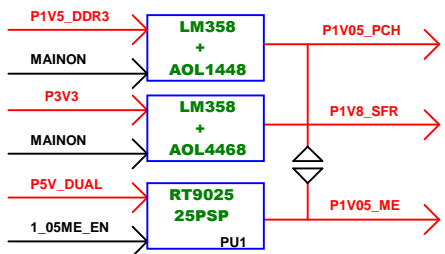
## P1V1\_VTT



**VCCSA**

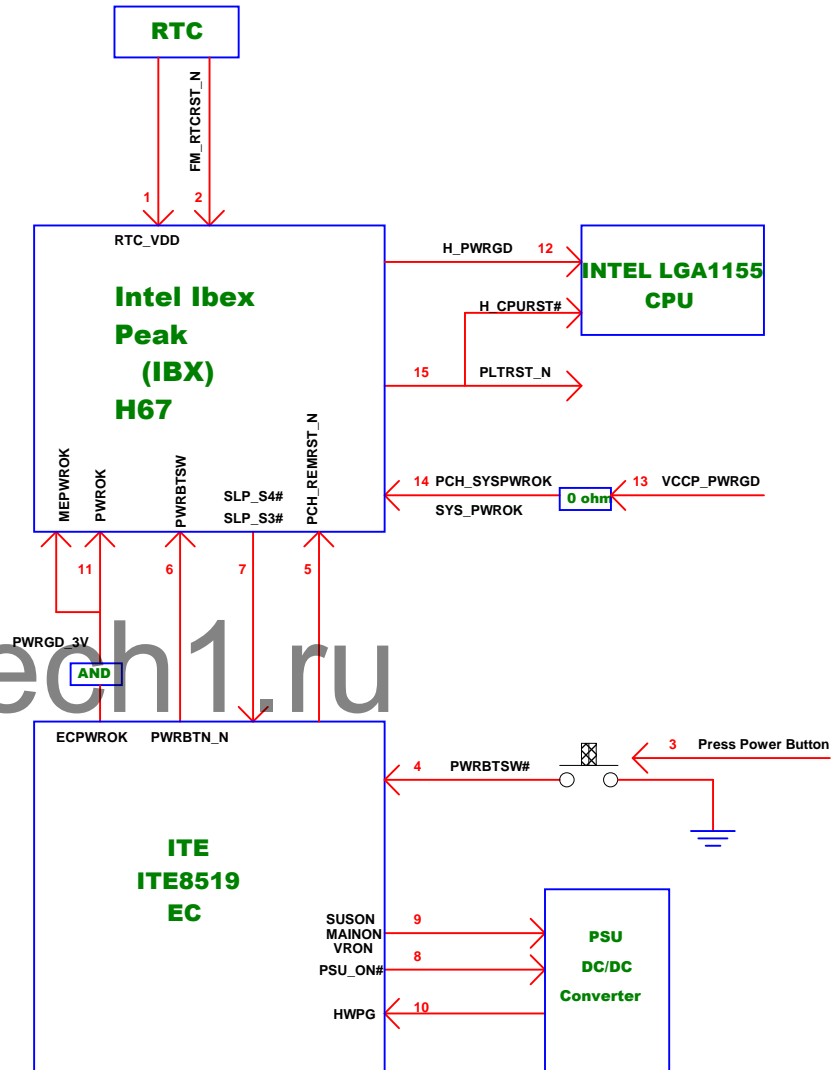


P1V05\_PCH/P1V8\_SFR/P1V05\_ME

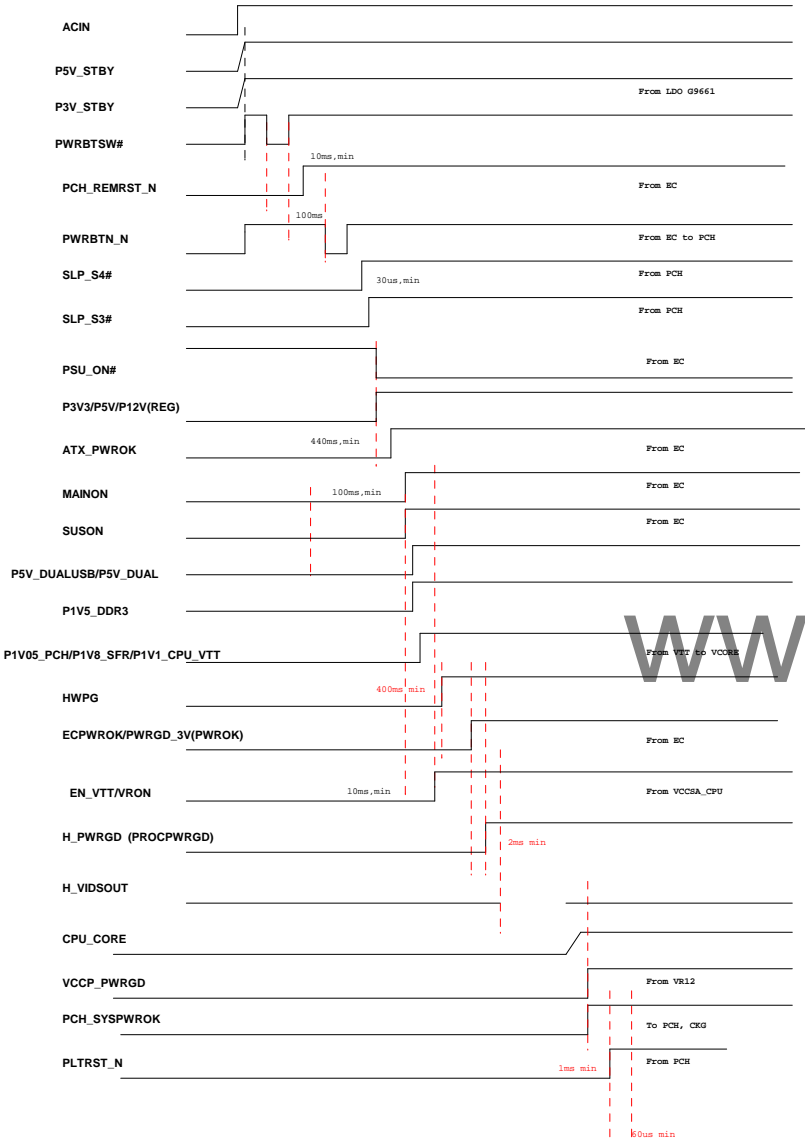


## Power on Sequence

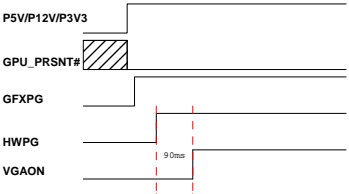
2



Power on Sequence :



MXM POWER ON



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(10,11) M\_A\_DQ[63:0]

M\_A\_A[15:0] (10,11)

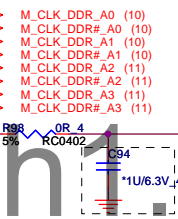
(10,11) M\_A\_DQS0  
(10,11) M\_A\_DQS1  
(10,11) M\_A\_DQS2  
(10,11) M\_A\_DQS3  
(10,11) M\_A\_DQS4  
(10,11) M\_A\_DQS5  
(10,11) M\_A\_DQS6  
(10,11) M\_A\_DQS7  
  
(10,11) M\_A\_DQS#0  
(10,11) M\_A\_DQS#1  
(10,11) M\_A\_DQS#2  
(10,11) M\_A\_DQS#3  
(10,11) M\_A\_DQS#4  
(10,11) M\_A\_DQS#5  
(10,11) M\_A\_DQS#6  
(10,11) M\_A\_DQS#7

M\_A\_DQS0 AK3  
M\_A\_DQS1 AP3  
M\_A\_DQS2 AW4  
M\_A\_DQS3 AV8  
M\_A\_DQS4 AV37  
M\_A\_DQS5 AP38  
M\_A\_DQS6 AK38  
M\_A\_DQS7 AF38  
  
M\_A\_DQS#0 AK2C  
M\_A\_DQS#1 AP2C  
M\_A\_DQS#2 AV4C  
M\_A\_DQS#3 AW8C  
M\_A\_DQS#4 AV36C  
M\_A\_DQS#5 AP39C  
M\_A\_DQS#6 AK39C  
M\_A\_DQS#7 AF39C

CN7A  
SA\_DQ0  
SA\_MA\_1  
SA\_DQ2  
SA\_DQ3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14  
SA\_MA\_15  
SA\_WE\_N  
SA\_CAS\_N  
SA\_RAS\_N  
SA\_BS0  
SA\_BS1  
SA\_BS2  
SA\_CS\_N0  
SA\_CS\_N1  
SA\_CS\_N2  
SA\_CS\_N3  
SA\_CKE0  
SA\_CKE1  
SA\_CKE2  
SA\_CKE3  
SA\_ODT0  
SA\_ODT1  
SA\_ODT2  
SA\_ODT3  
SA\_CLK\_N0  
SA\_CLK\_N1  
SA\_CLK\_N2  
SA\_CLK\_N3  
SM\_DRAMRST\_N  
SA\_DQS\_8  
SA\_DQS\_N\_8  
SA\_ECC\_CB0  
SA\_ECC\_CB1  
SA\_ECC\_CB2  
SA\_ECC\_CB3  
SA\_ECC\_CB4  
SA\_ECC\_CB5  
SA\_ECC\_CB6  
SA\_ECC\_CB7  
SA\_DQS\_N\_0  
SA\_DQS\_N\_1  
SA\_DQS\_N\_2  
SA\_DQS\_N\_3  
SA\_DQS\_N\_4  
SA\_DQS\_N\_5  
SA\_DQS\_N\_6  
SA\_DQS\_N\_7

SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14  
SA\_MA\_15  
SA\_WE\_N  
SA\_CAS\_N  
SA\_RAS\_N  
SA\_BS0  
SA\_BS1  
SA\_BS2  
SA\_CS\_N0  
SA\_CS\_N1  
SA\_CS\_N2  
SA\_CS\_N3  
SA\_CKE0  
SA\_CKE1  
SA\_CKE2  
SA\_CKE3  
SA\_ODT0  
SA\_ODT1  
SA\_ODT2  
SA\_ODT3  
SA\_CLK\_N0  
SA\_CLK\_N1  
SA\_CLK\_N2  
SA\_CLK\_N3  
SM\_DRAMRST\_N  
SA\_DQS\_8  
SA\_DQS\_N\_8  
SA\_ECC\_CB0  
SA\_ECC\_CB1  
SA\_ECC\_CB2  
SA\_ECC\_CB3  
SA\_ECC\_CB4  
SA\_ECC\_CB5  
SA\_ECC\_CB6  
SA\_ECC\_CB7  
SA\_DQS\_N\_0  
SA\_DQS\_N\_1  
SA\_DQS\_N\_2  
SA\_DQS\_N\_3  
SA\_DQS\_N\_4  
SA\_DQS\_N\_5  
SA\_DQS\_N\_6  
SA\_DQS\_N\_7

AV27 M\_A\_A0  
AY24 M\_A\_A1  
AW24 M\_A\_A2  
AW23 M\_A\_A3  
AV23 M\_A\_A4  
AT24 M\_A\_A5  
AT23 M\_A\_A6  
AV22 M\_A\_A7  
AV22 M\_A\_A8  
AT22 M\_A\_A9  
AV26 M\_A\_A10  
AU21 M\_A\_A11  
AT21 M\_A\_A12  
AW32 M\_A\_A13  
AU20 M\_A\_A14  
AT20 M\_A\_A15  
AW29 M\_A\_WE#  
AV30 M\_A\_CAS#  
AU28 M\_A\_RAS#  
AY29 M\_BA\_A0  
AW28 M\_BA\_A1  
AV20 M\_BA\_A2  
AU29 M\_CS#\_A0  
AV32 M\_CS#\_A1  
AW30 M\_CS#\_A2  
AU33 M\_CS#\_A3  
AV19 M\_CKE\_A0  
AT19 M\_CKE\_A1  
AU18 M\_CKE\_A2  
AV18 M\_CKE\_A3  
AV31 M\_ODT\_A0  
AU32 M\_ODT\_A1  
AU30 M\_ODT\_A2  
AW33 M\_ODT\_A3  
AY25 M\_CLK\_DDR\_A0  
AW25 M\_CLK\_DDR#\_A0  
AU24 M\_CLK\_DDR\_A1  
AU25 M\_CLK\_DDR#\_A1  
AW27 M\_CLK\_DDR#\_A2  
AV26 M\_CLK\_DDR\_A3  
AW26 M\_CLK\_DDR#\_A3  
AW18 DDR3\_DRAMRST\_N R  
OR 4  
RC0402  
C64  
\*1U6.3V\_4  
AV13 M\_A\_DQS8  
AV12 M\_A\_DQS#8  
AU12  
AU14  
AW13  
AY13  
AU13  
AU11  
AY12  
AW12



DDR3\_DRAMRST# (10,11,12,13)

DDR\_0

LGA1155

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PROJECT: QK1

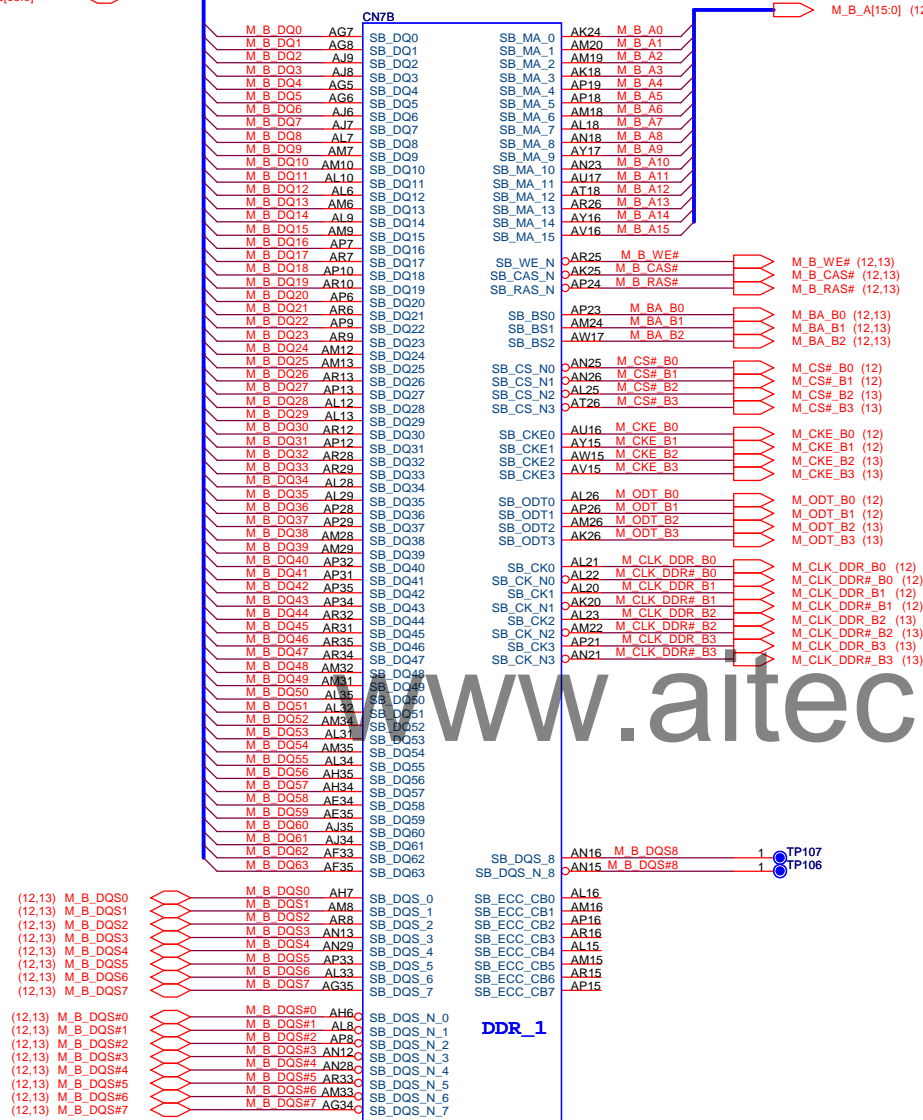
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SOCKET H2 DDR3 CHANNEL A	A
Date:	Friday, April 15, 2011	Sheet 4 of 44



(12,13) M\_B\_DQ[63:0]

M\_B\_A[15:0] (12,13)



CN7B

LGA1155

DDR\_1

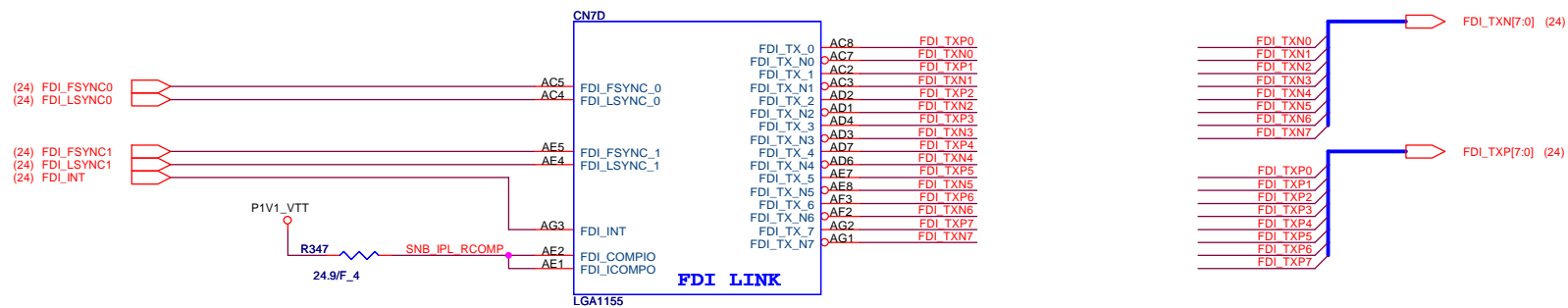
PROPRIETARY NOTE  
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PROJECT: QK1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SOCKET H2 DDR3 CHANNEL B	A
Date:	Friday, April 15, 2011	Sheet 5 of 44

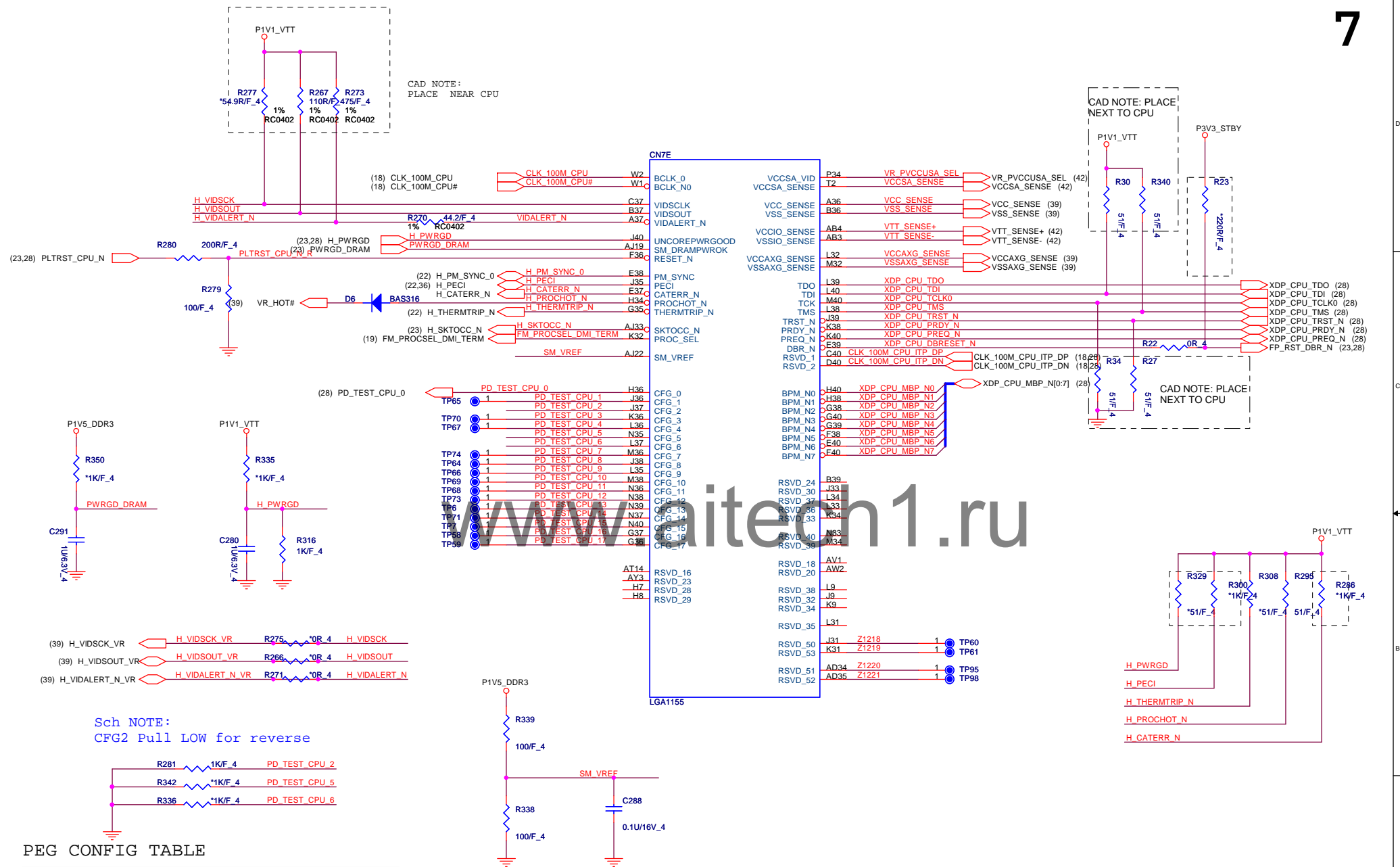


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**PROJECT : QK1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	SOCKET H2 PCIE, DMI	A
Date:	Friday, April 15, 2011	Sheet 6 of 44

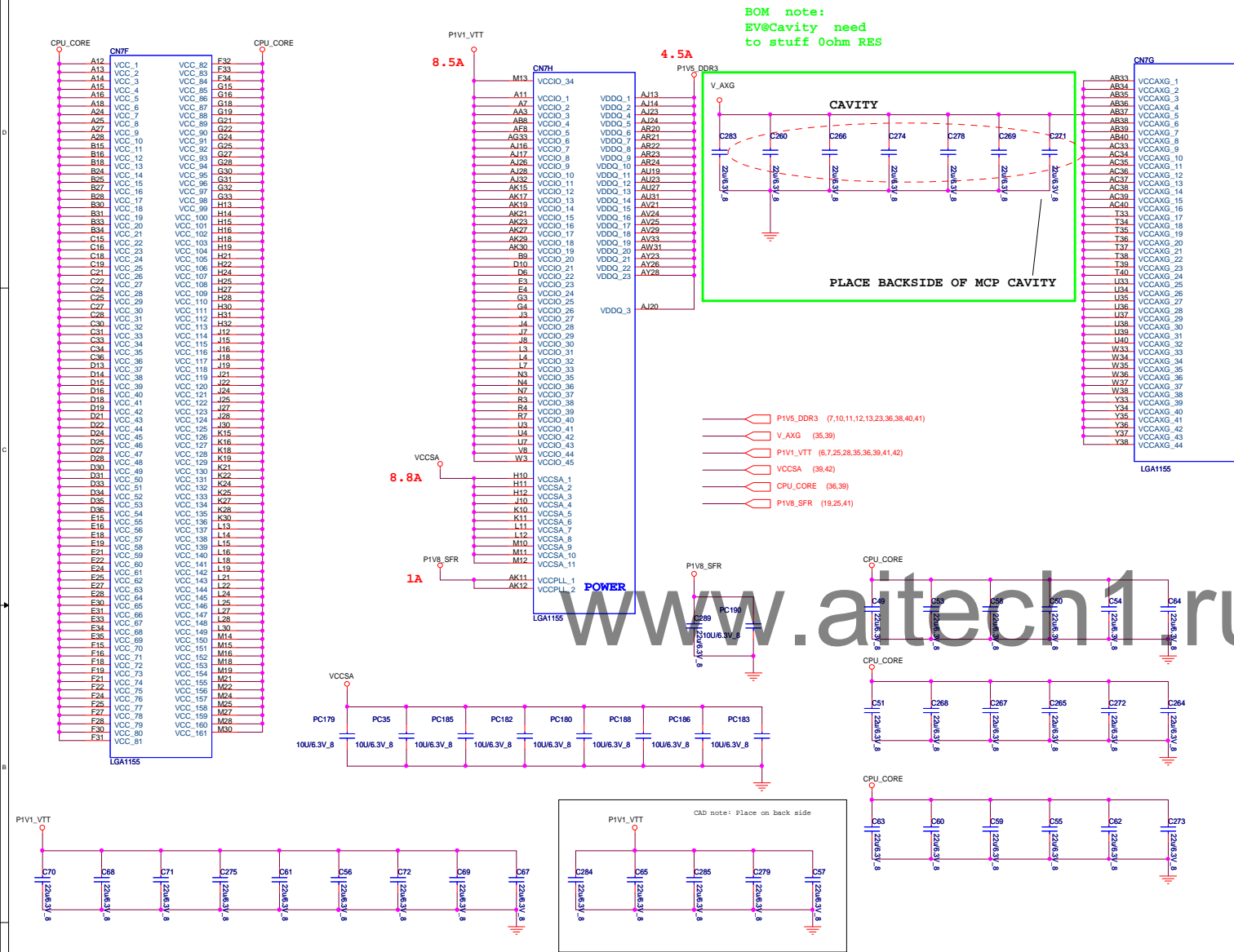


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PROJECT: QK1  
Quanta Computer Inc.

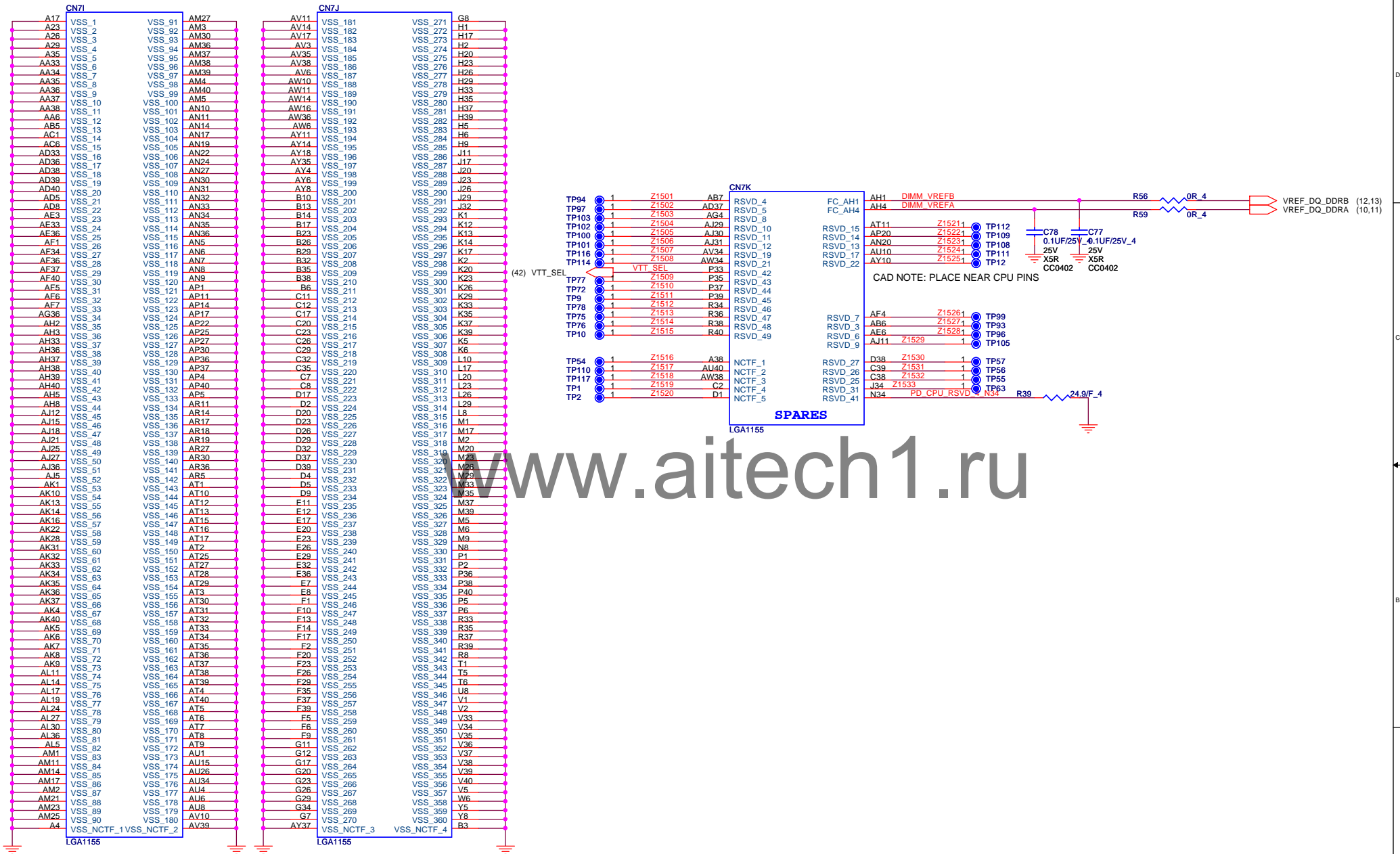
Size	Document Number	Rev
Custom	SOCKET H2 CLK, CTRL, MISC, DE	A
Date:	Friday, April 15, 2011	Sheet 7 of 44

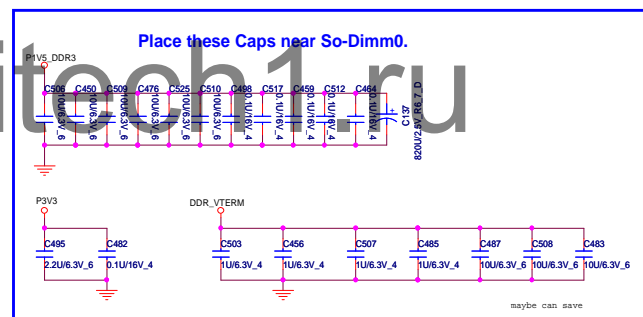
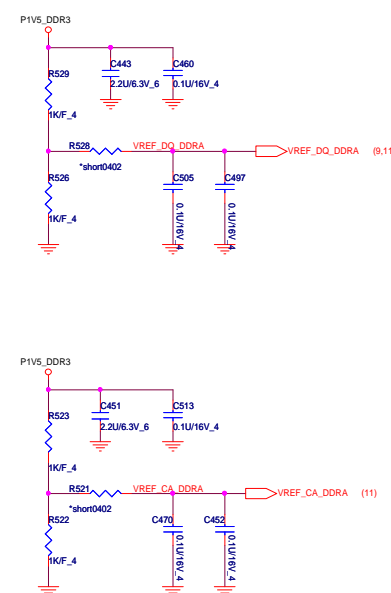
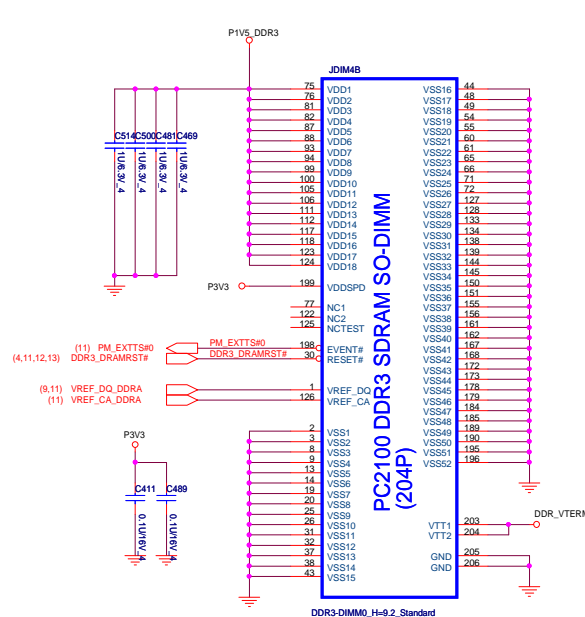
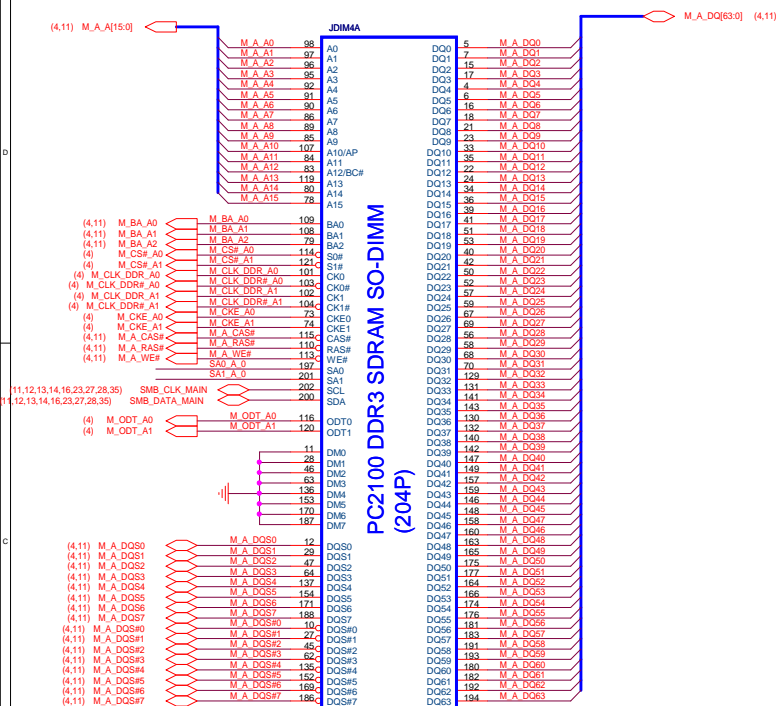


## DESIGN NOTE:

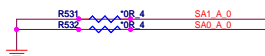
NET	PROCESSOR
VCCP	SVID
V_AXG	SVID
PVCCP_CPU	1.05V/1.00V
PVCCUSA_CPU	0.925V/0.85V
PIV5_DDR3	1.5V
PIV8_SFR	1.8V

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SPD SA0	0
SPD SA1	0



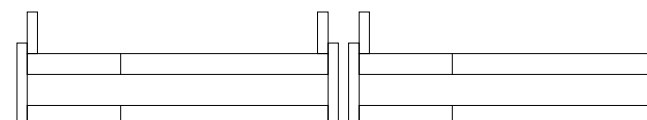
FOX H:9.2 white  
PCB Placement

STD: EL2C

DGMK4000109	5.2mm 01:ddr-as0a626-n2sn-7h-204p-ldv
DGMK4000116	9.2mm 00:ddr-as0a626-iasq-7h-204p-ldv

11: 5.2mm DIMM 3

10: 9.2mm DIMM 4



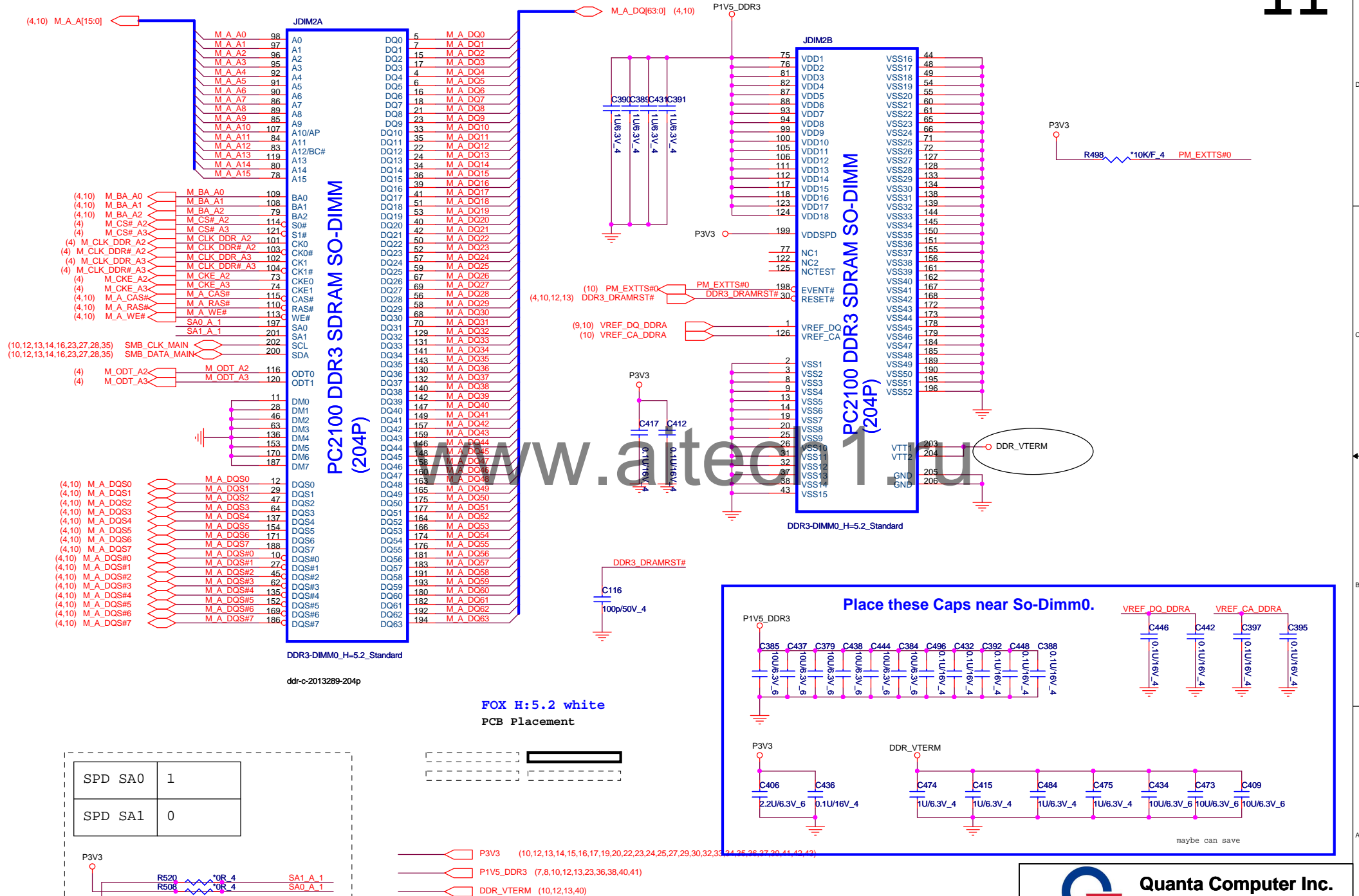
```
01: 5.2mm  DIMM 1
```

```
00: 9.2mm DIMM 2
```

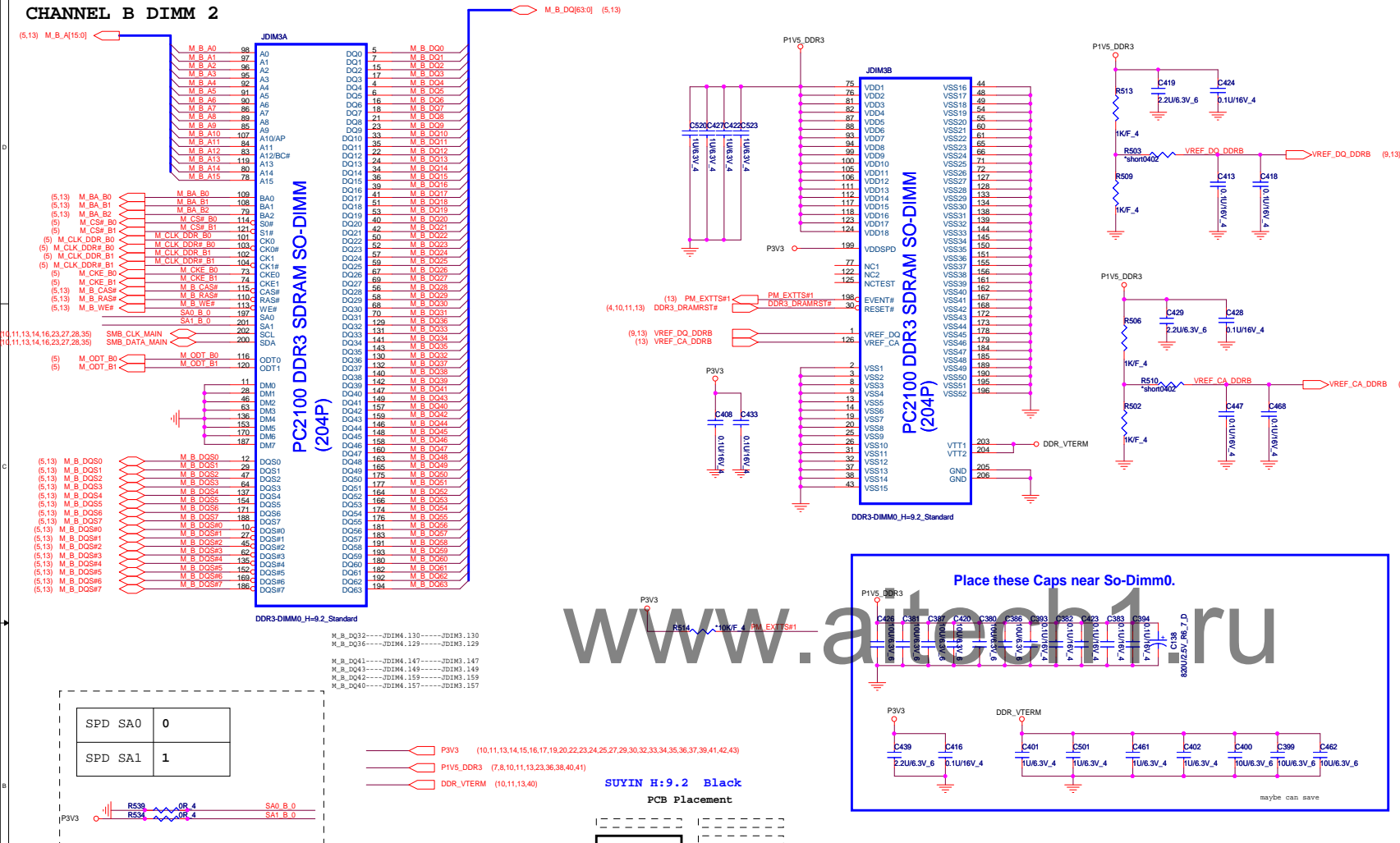


# CHANNEL A DIMM 1

11



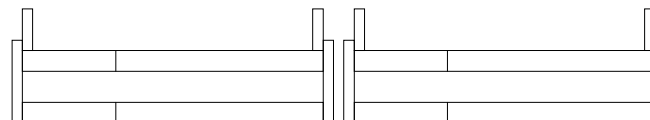
## CHANNEL B DIMM 2



STD: EL2C

DGMK4000109	DGMK4000155	5.2mm 01:ddr-as0a626-n2sn-7h-204p-ldv
DGMK4000116	DGMK4000157	9.2mm 00:ddr-as0a626-jasg-7h-204p-ldv

```
11: 5.2mm    DIMM 3
10: 9.2mm    DIMM 4
```

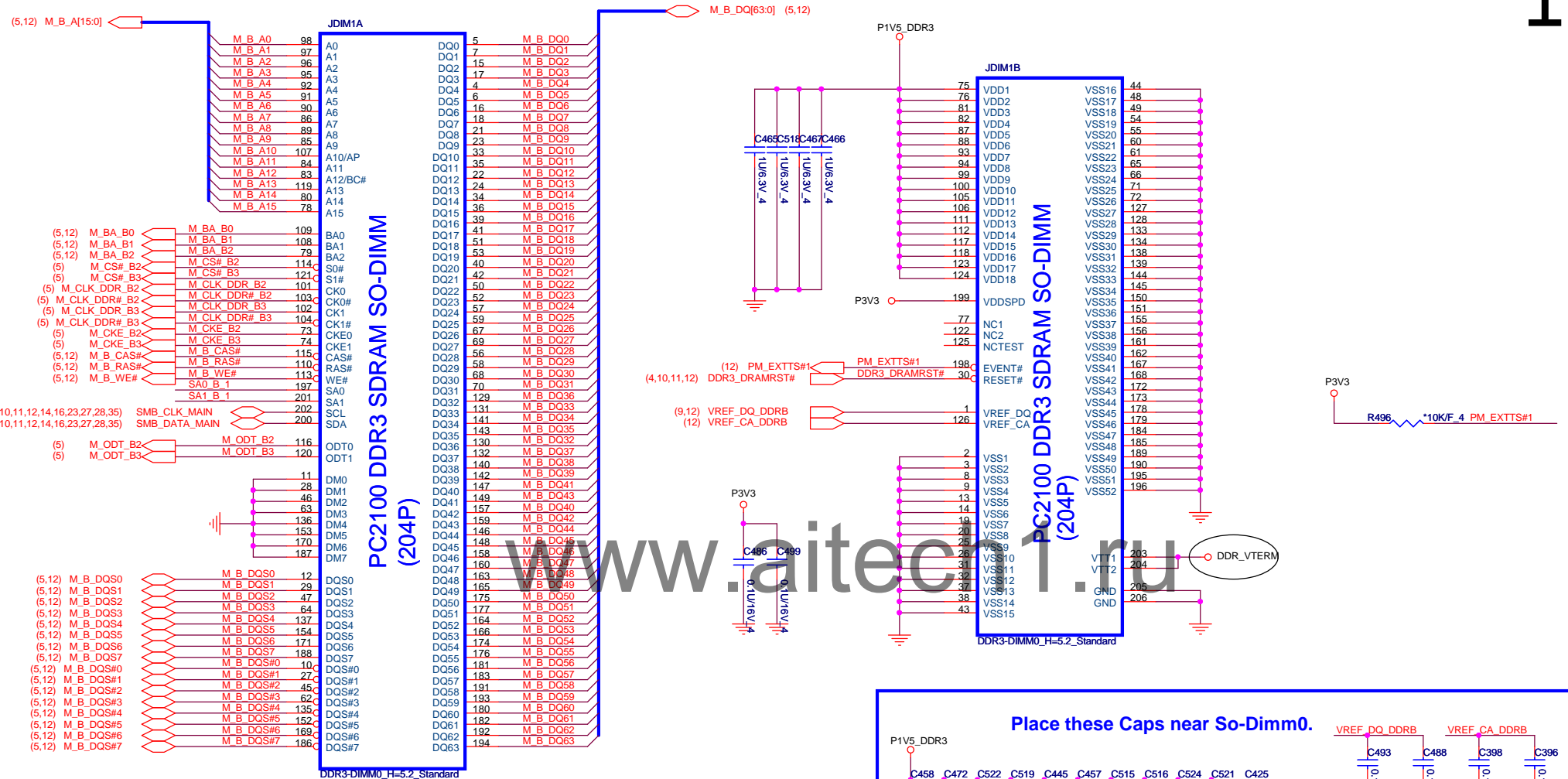


```
01: 5.2mm    DIMM 1
00: 9.2mm    DIMM 2
```

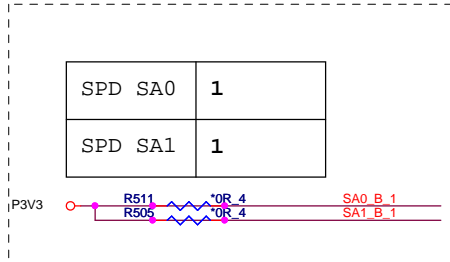


# CHANNEL B DIMM 3

13



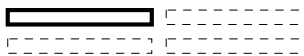
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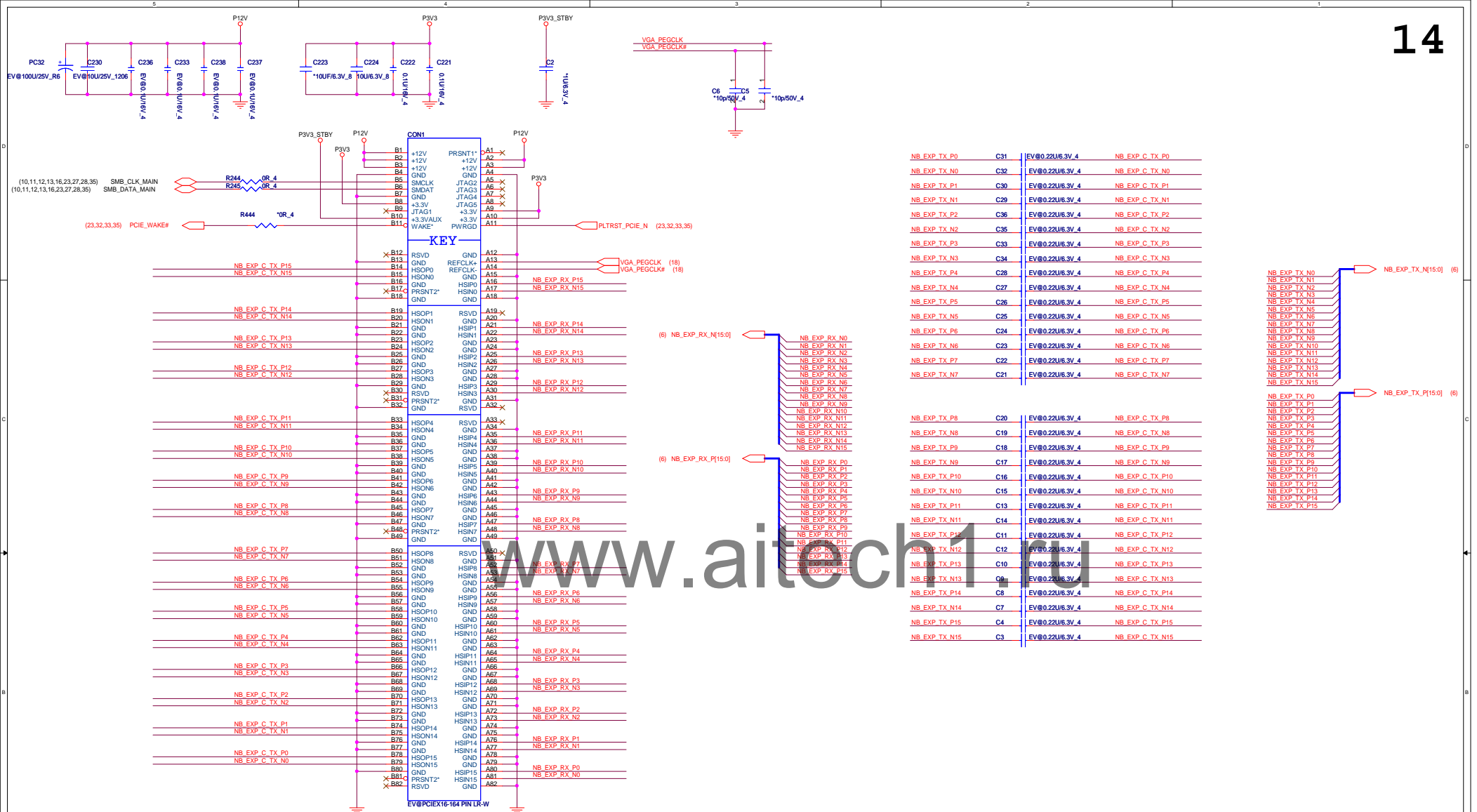
STD: EL2C  
DGMK4000109  
DGMK4000116

SUYIN H:5.2 Black

PCB Placement

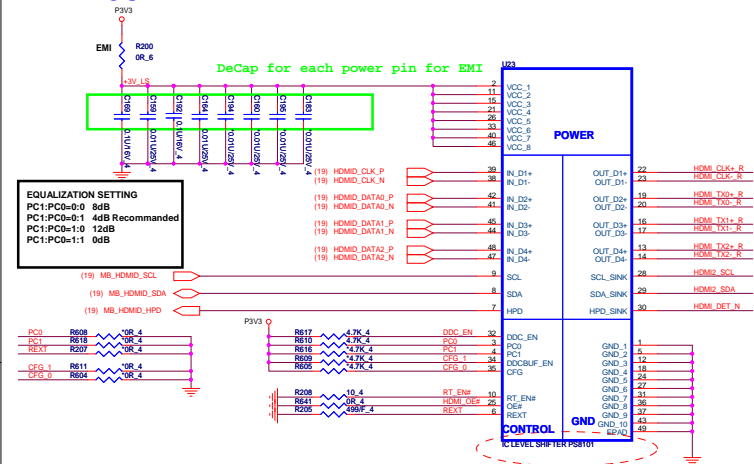


- P3V3 (10,11,12,14,15,16,17,19,20,22,23,24,25,27,29,30,32,33,34,35,36,37,39,41,42,43)
- P1V5\_DDR3 (7,8,10,11,12,23,36,38,40,41)
- DDR\_VTERM (10,11,12,40)





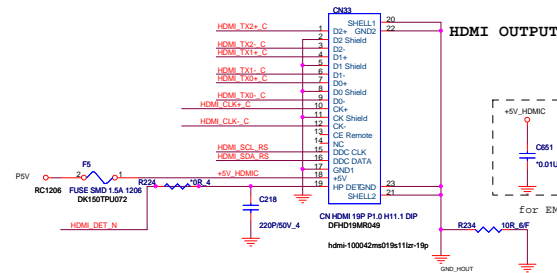
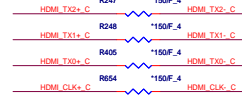




Mount for Non-EXT\_VGA Option.



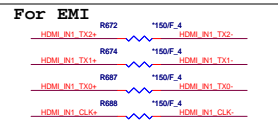
For EM



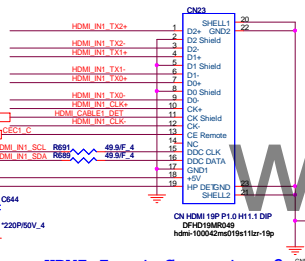
Mount for Non-EXT\_VGA Option.



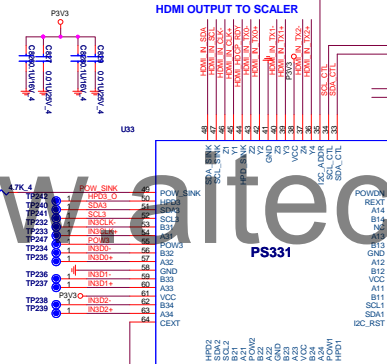
## HDMI INPUT CONN



## HDMI Input Connector

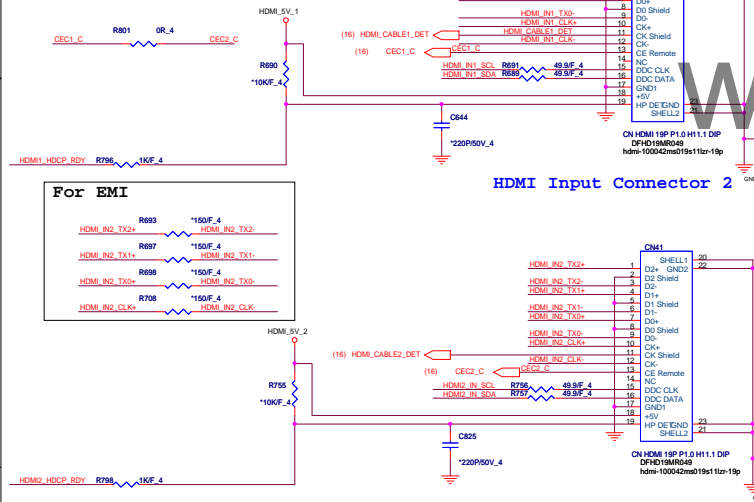
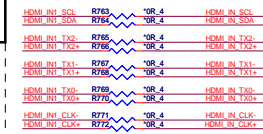


## HDMI INPUT SWITCH IC



DEVICE ADDRESS:  
I2C\_ADDR=0 -> Control Register: 94/95, EDID Shadow: 96/97  
I2C\_ADDR=1 -> Control Register: B4/B5, EDID Shadow: B6/B7

ONLY 1 PORT HDMI INPUT



NOTE:  
For each port, 4 pairs of TMD5 input pins (Axy / Bxy ) are designed identical  
So TMD5 CLK<sup>+</sup>/<sub>-</sub> and Data<sup>+</sup>/<sub>-</sub> can be connected freely to any pair of TMD5 input pins  
Also positive and negative can be swapped for each pair TMD5 input pins  
It's the same for PS331 4 pairs of TMD5 output pins (Yy/Zy)

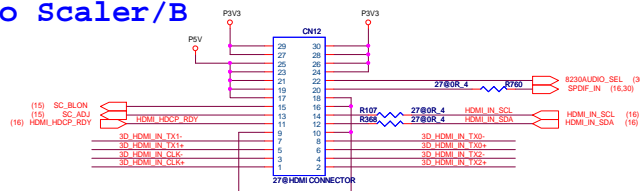
## HDMI INPUT

Closed CN12



HDMI input and Scalar/B control

## HDMI INPUT to Scaler/B



COPY FROM LVDS CONN 30P



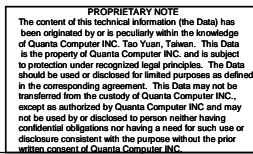
NOTE:  
RESISTORS NEAR CPU AND XDP HEADER AND OVERLAP COMMON PAD

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Rev  
A

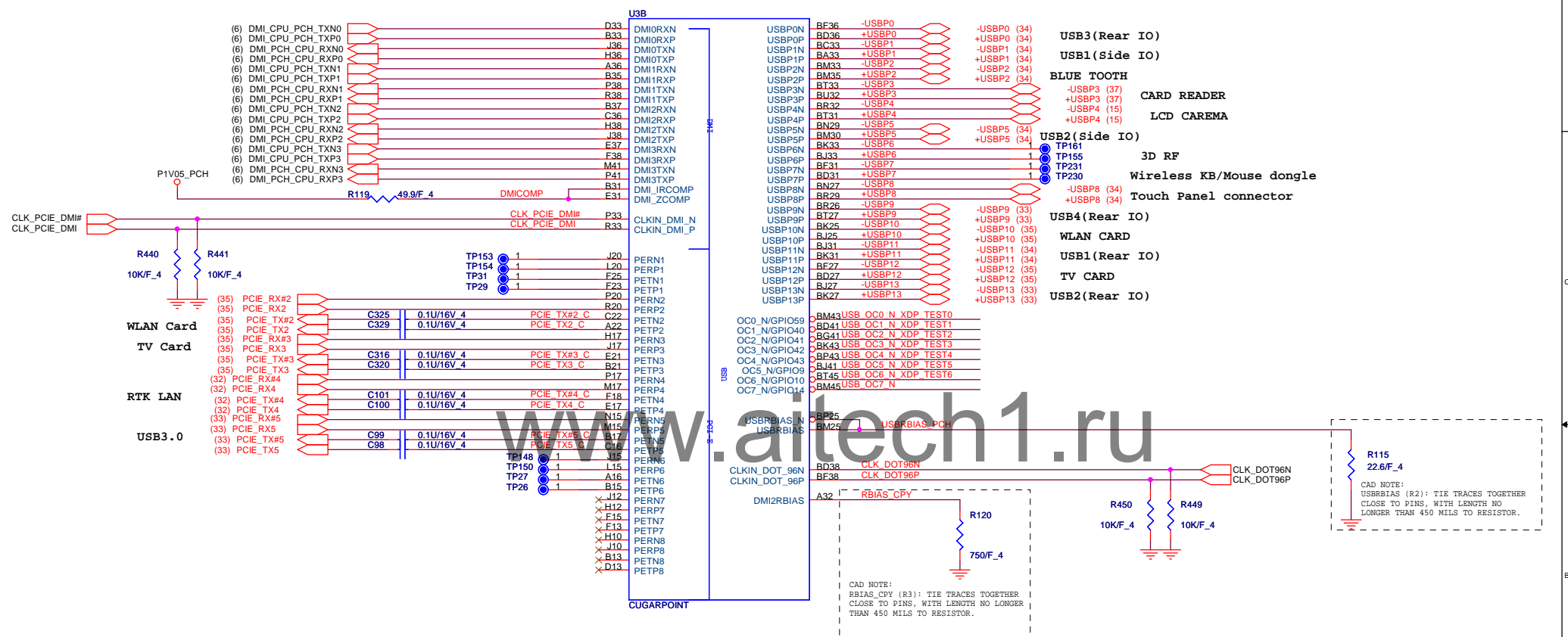
Date: Friday, April 15, 2011 Sheet 18 of 44

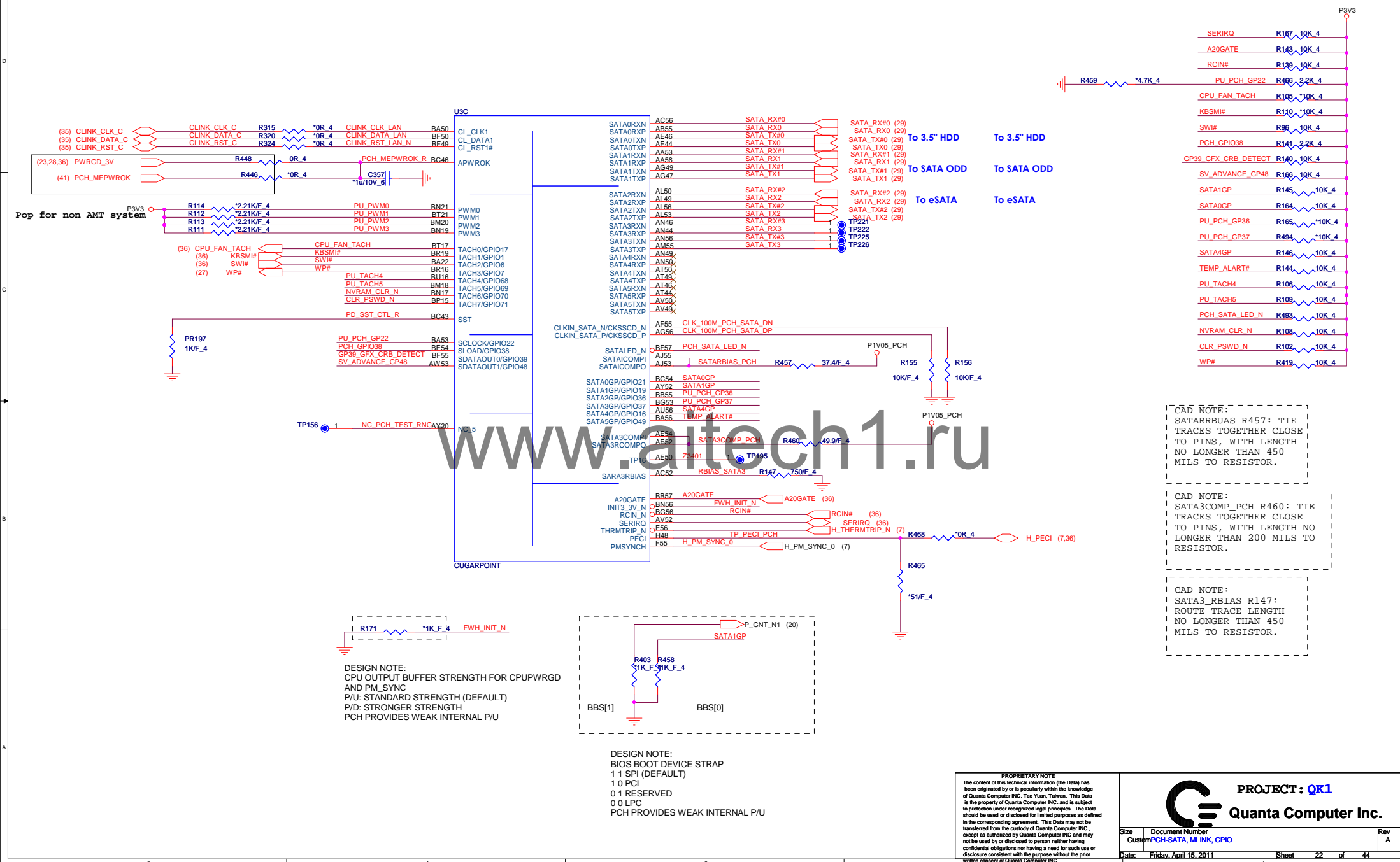


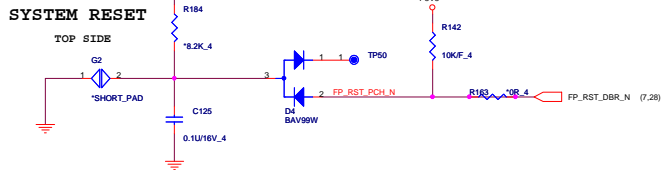
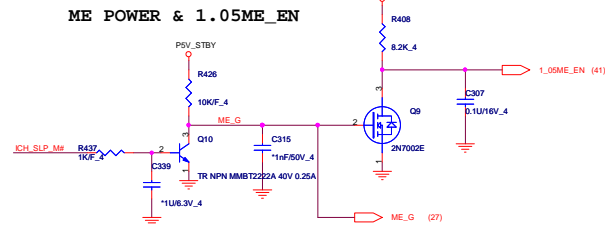
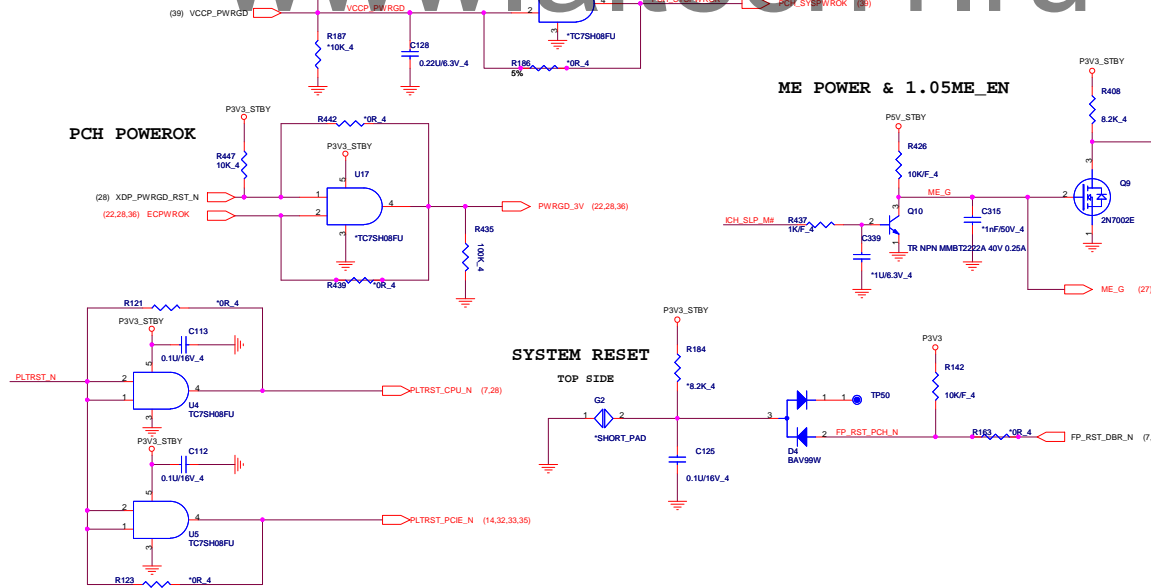
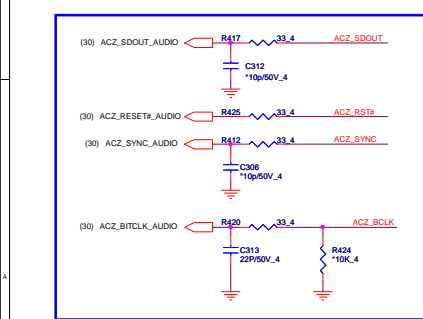
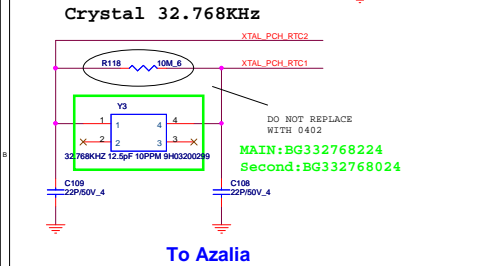
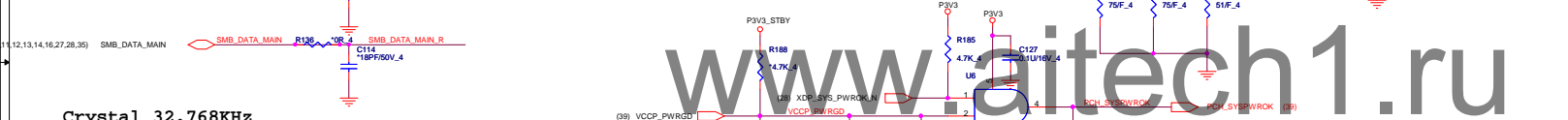
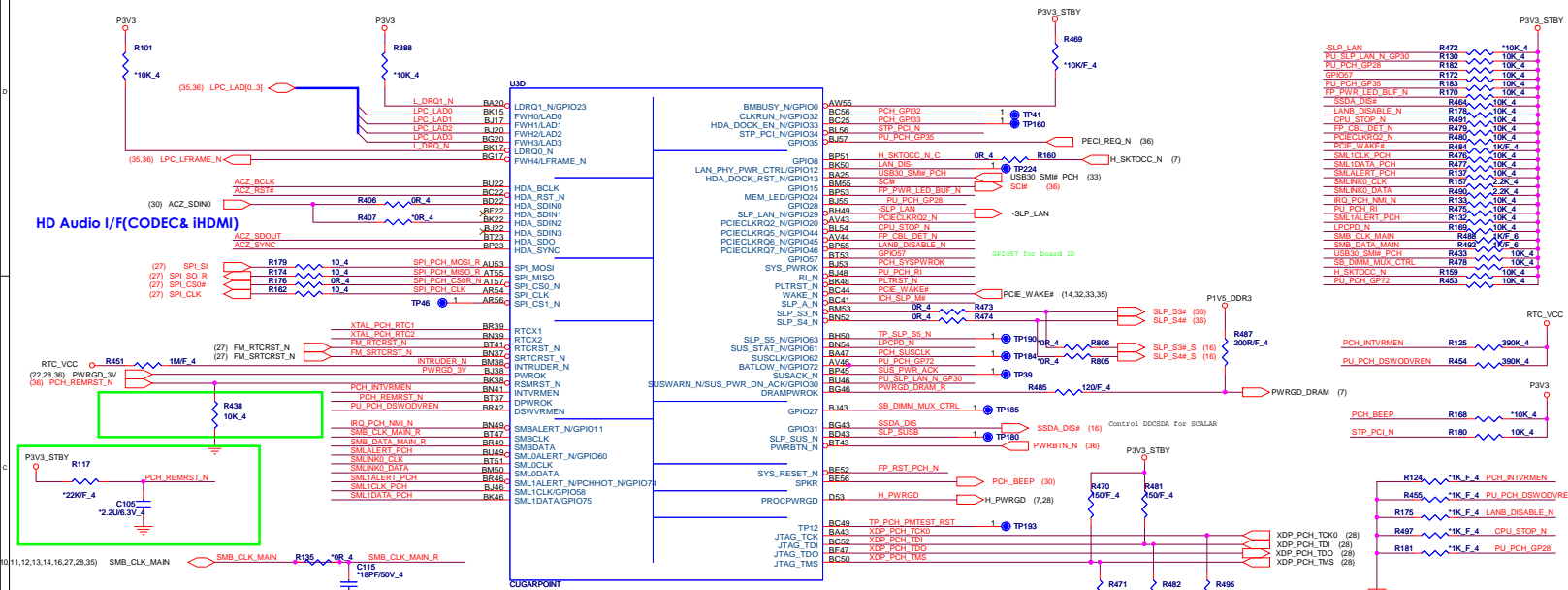


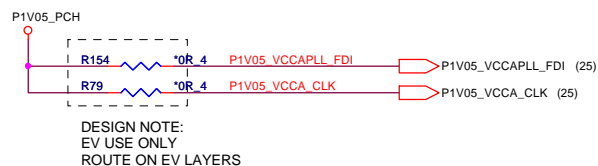
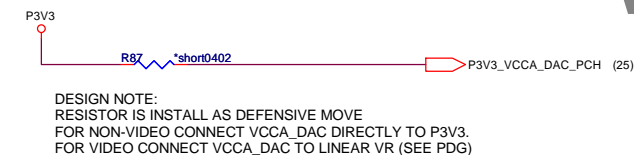
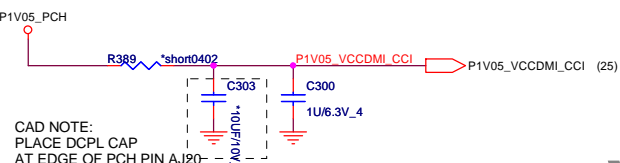
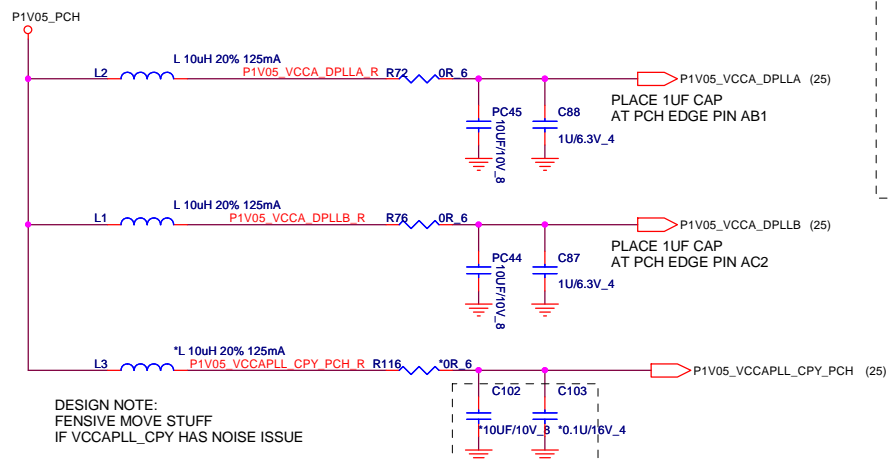






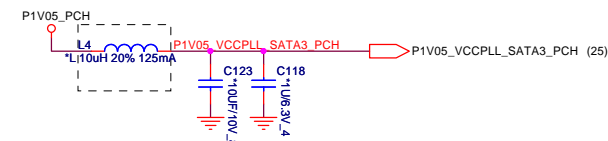




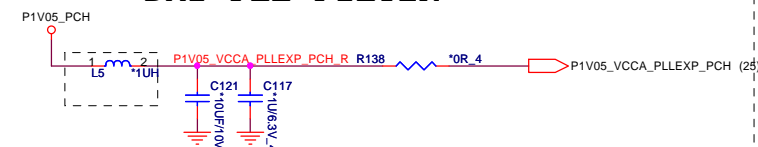


### SATA PLL FILTER

CAD NOTE:  
PLACE VCCSATA DCPL CAPS AT ENDS OF POWER CORRIDOR



### DMI PLL FILTER



CAD NOTE:  
PLACE VCCAPLEXP CAPS AT ENDS OF POWER CORRIDOR

DESIGN NOTE:  
DEFENSIVE EXTERNAL SOURCE FOR VCCAPLL\_EXP

www.aitech1.ru

TP169	1	Z3601	H31
TP38	1	Z3602	J31
TP37	1	Z3603	C29
TP36	1	Z3604	E29
TP167	1	Z3605	J27
TP170	1	Z3606	L27
TP33	1	Z3607	E28
TP34	1	Z3608	E27
TP162	1	Z3609	J25
TP163	1	Z3610	L25
TP32	1	Z3611	C26
TP35	1	Z3612	B27
TP159	1	Z3613	L22
TP158	1	Z3614	J22
TP28	1	Z3615	B25
TP30	1	Z3616	D25

U3G

FDI_RXN0	C42	FDI_TXN0
FDI_RXP0	B43	FDI_TXP0
FDI_RXN1	F45	FDI_TXN1
FDI_RXP1	F43	FDI_TXP1
FDI_RXN2	H41	FDI_TXN2
FDI_RXP2	J41	FDI_TXP2
FDI_RXN3	C46	FDI_TXN3
FDI_RXP3	D47	FDI_TXP3
FDI_RXN4	B45	FDI_TXN4
FDI_RXP4	A46	FDI_TXP4
FDI_RXN5	B47	FDI_TXN5
FDI_RXP5	C49	FDI_TXP5
FDI_RXN6	J43	FDI_TXN6
FDI_RXP6	H43	FDI_TXP6
FDI_RXN7	M43	FDI_TXN7
FDI_RXP7	P43	FDI_TXP7
FDI_FSYNC0	B51	FDI_FSYNC0 (6)
FDI_LSYNC0	E49	FDI_LSYNC0 (6)
FDI_FSYNC1	C52	FDI_FSYNC1 (6)
FDI_LSYNC1	D51	FDI_LSYNC1 (6)
FDI_INT	H46	FDI_INT (6)

FDI\_TXN[7:0] (6)

FDI\_TXP[7:0] (6)

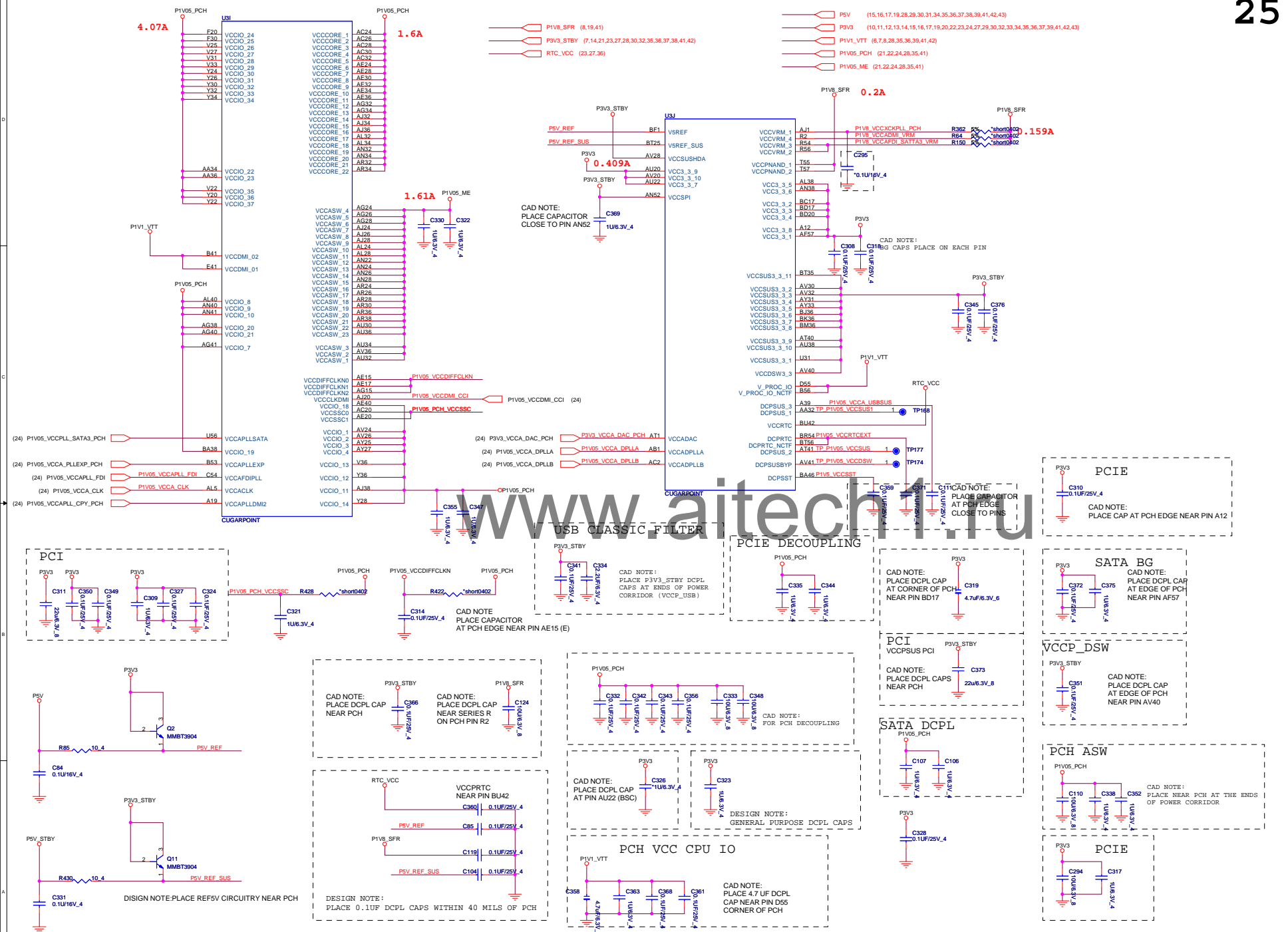
#### PROPRIETARY NOTE

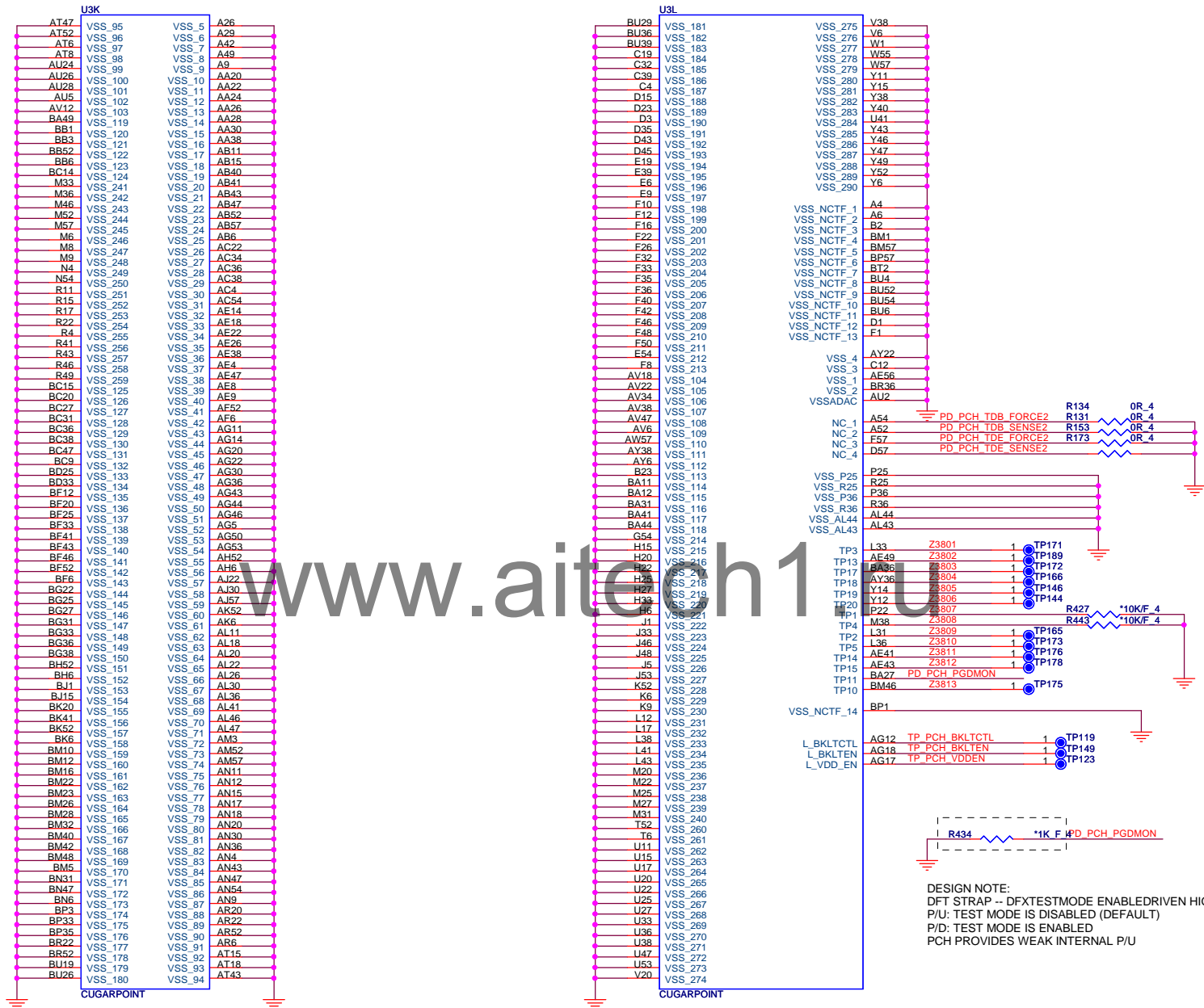
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PROJECT: QK1  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH-PLL FILTERS	A
Date:	Friday, April 15, 2011	Sheet 24 of 44





DESIGN NOTE:  
 DFT STRAP -- DFTTESTMODE ENABLEDRIVEN HIGH OR LOW  
 P/U: TEST MODE IS DISABLED (DEFAULT)  
 P/D: TEST MODE IS ENABLED  
 PCH PROVIDES WEAK INTERNAL P/U

**PROPRIETARY NOTE**  
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**PROJECT: QK1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	PCH-GND	A
Date:	Thursday, April 07, 2011	Sheet 26 of 44

BATTERY  
CR2032

CR2032  
+

Battery Part

[illegible][illegible]

CAD NOTE:  
PLACE 1UF CLOSE  
TO DIODE NEAR  
BATTERY HOLDER

[illegible]

---

PROPRIETARY NOTE

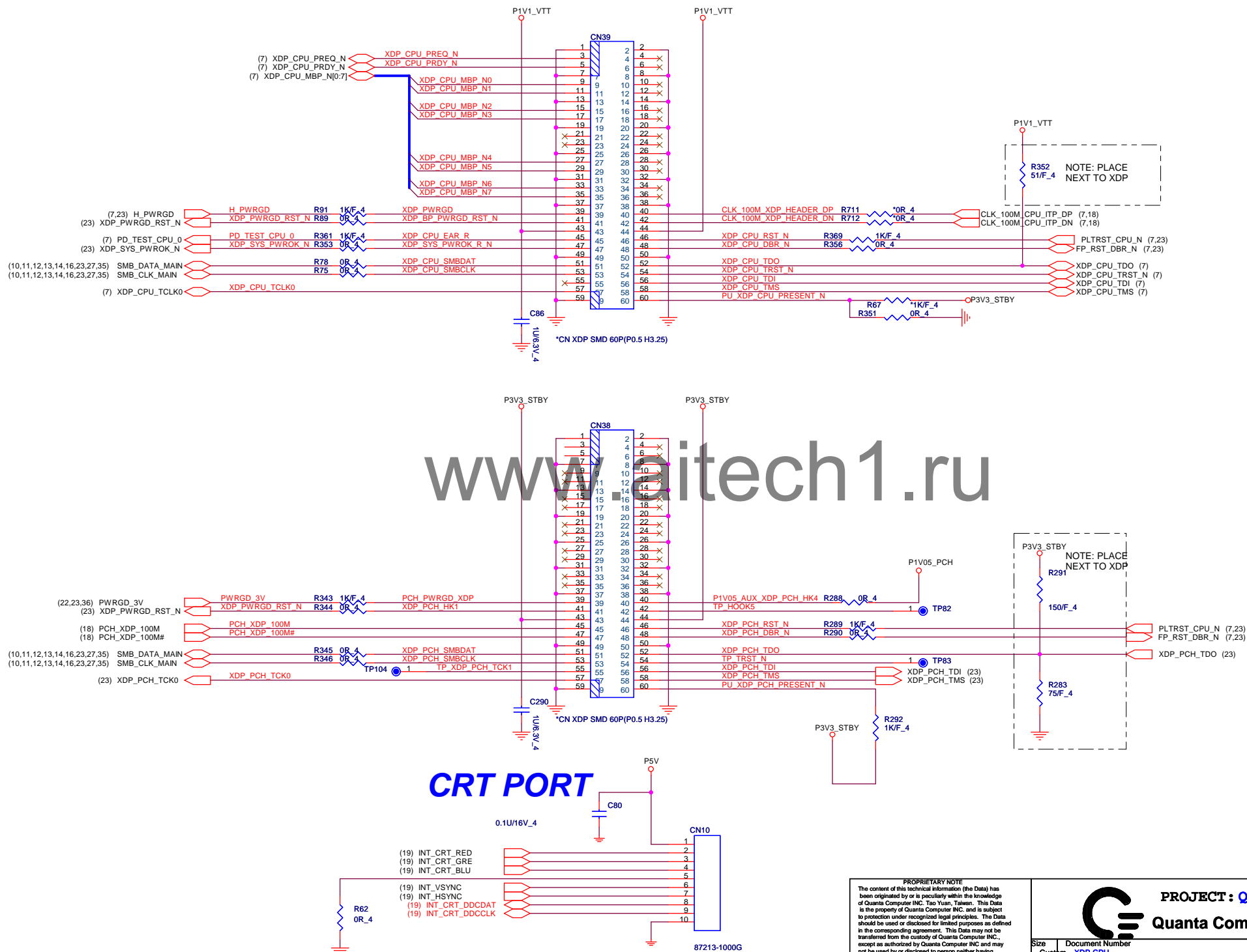
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PROJECT: QK1  
Quanta Computer Inc.

Size Custom	Document Number <b>RSM_RST AND BATTERY</b>	Rev A
Date: Friday, April 15, 2011	Sheet 27 of 44	





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**PROJECT: QK1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	XDP-CPU	A
Date:	Friday, April 15, 2011	Sheet 28 of 44



Check New ODD CONN Pin Define.

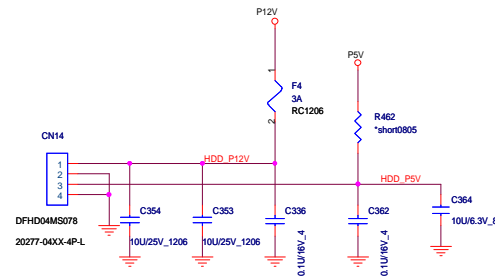
[illegible]

Diagram illustrating the connection between the SATA controller (CN25) and the SATA-Express connector (CN26).

The SATA controller (CN25) pins are connected to the SATA-Express connector (CN26) pins as follows:

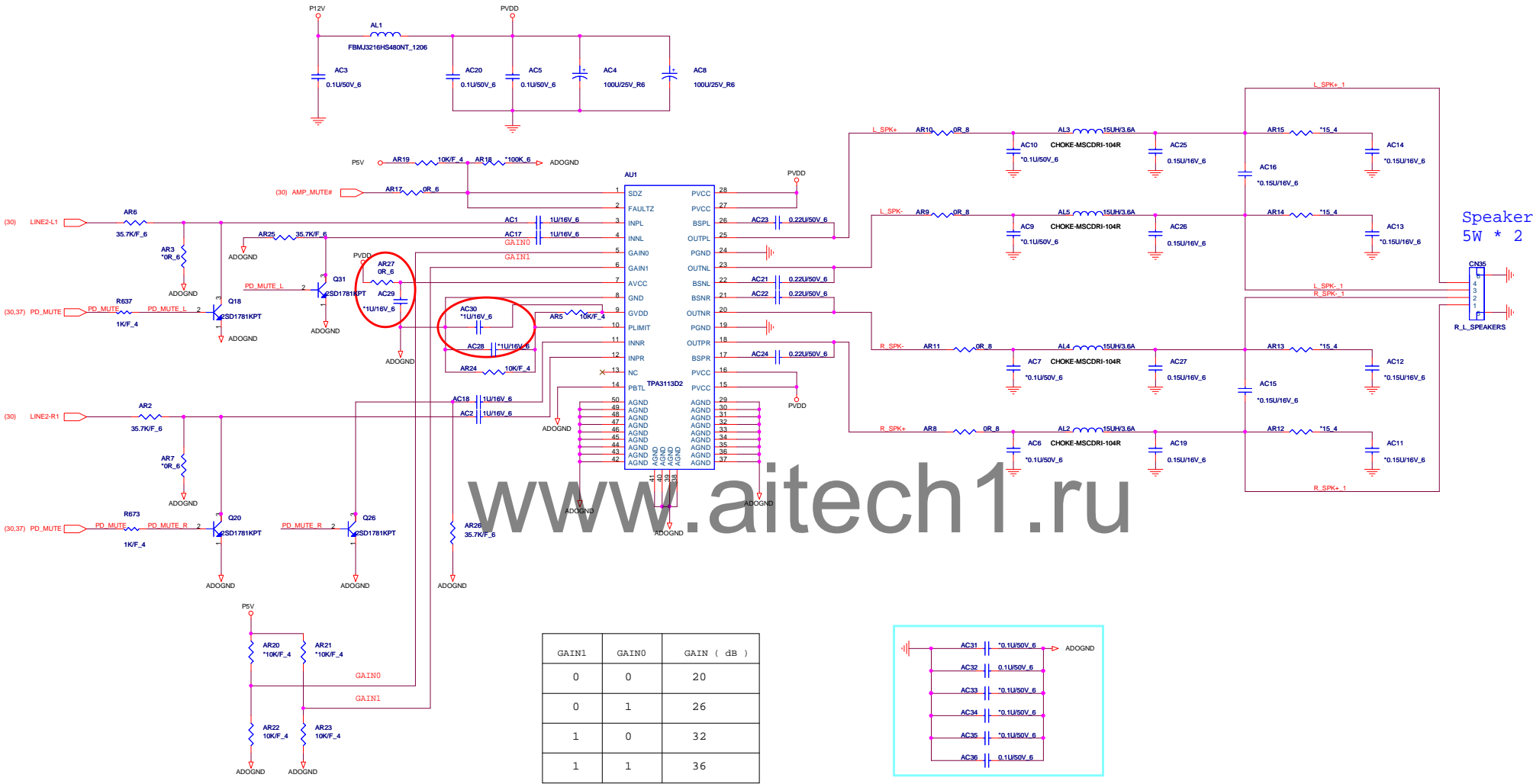
- GND1 (1) to GND4-GND3
- TXP (2) to SATA\_RD2\_TX (C631) with a 0.01u/25V 4 capacitor
- TXN (3) to SATA\_RD2\_TX# (C632) with a 0.01u/25V 4 capacitor
- GND2 (4) to GND4-GND3
- RXN (5) to SATA\_RD2\_RX# (C633) with a 0.01u/25V 4 capacitor
- RXP (6) to SATA\_RD2\_RX (C634) with a 0.01u/25V 4 capacitor
- GND4-GND3 (7) to GND4-GND3

The SATA-Express connector (CN26) is connected to the SATA-Express port (CN26) through a series of resistors and capacitors:

- R226 (10R, 0F) connects the SATA-Express port (CN26) to the SATA-Express connector (CN26).
- The SATA-Express connector (CN26) is connected to the SATA-Express port (CN26) through a series of resistors and capacitors.



Speaker AMP.





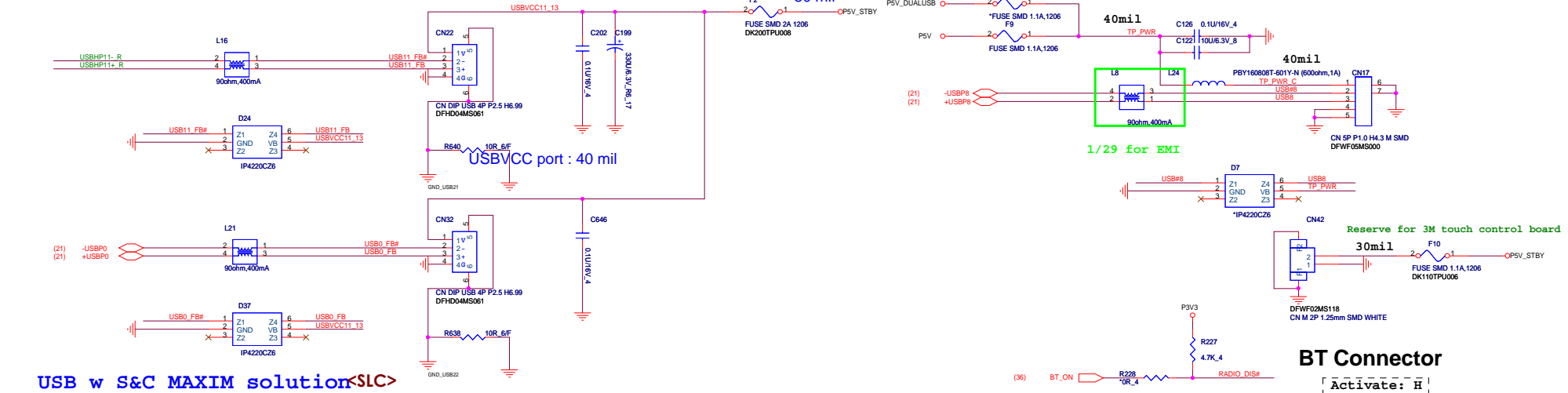


REAR USB PORT X4

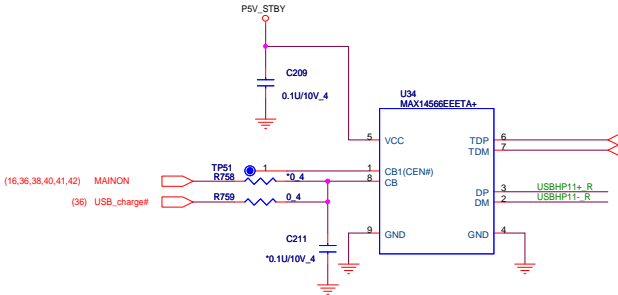
USBVCC port : 40 mil

Touch Panel connector

80 mil



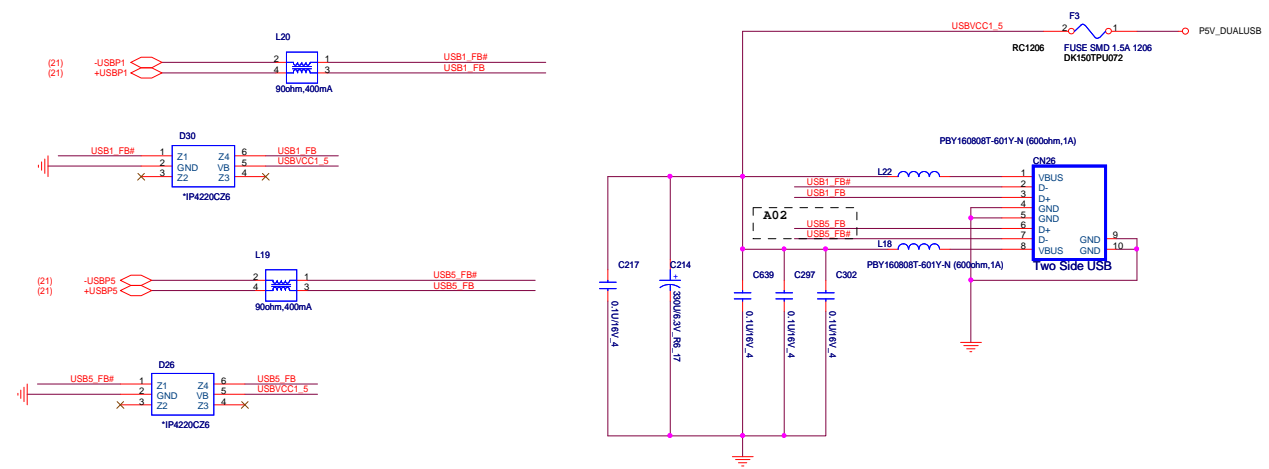
USB w S&C MAXIM solution<SLC>



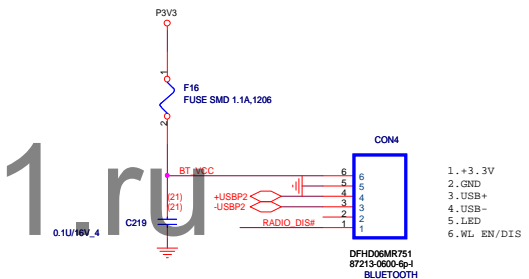
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

SIDE USB PORT X2

USBVCC port : 80 mil



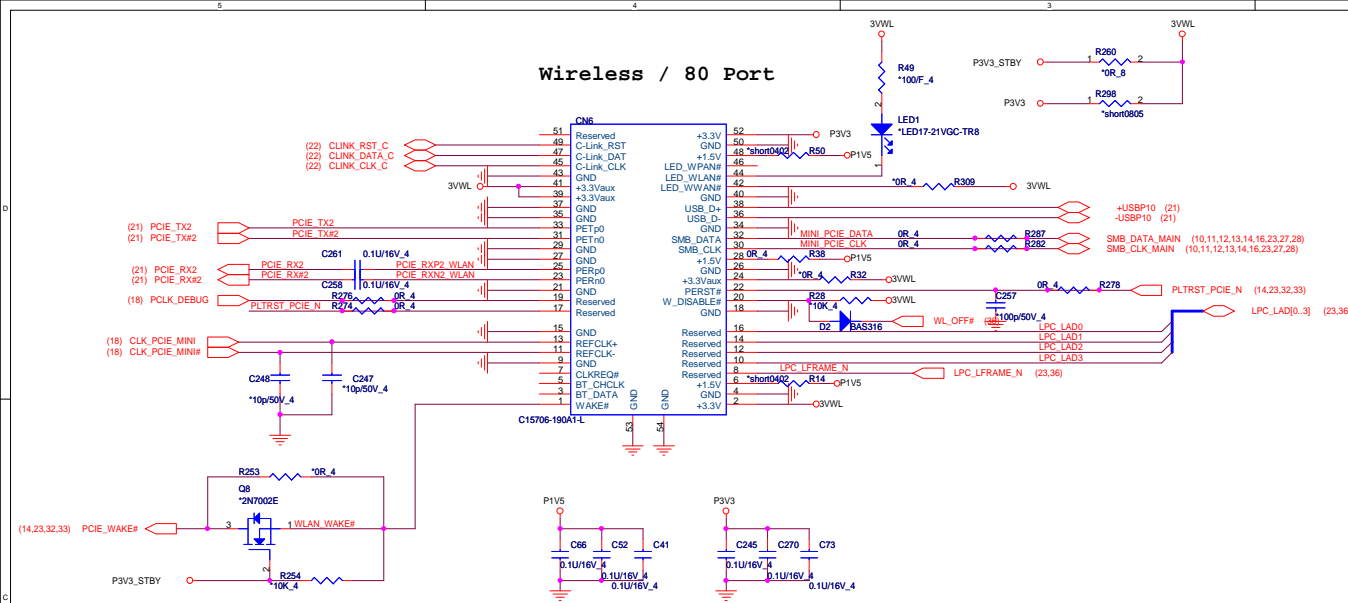
TOP Side



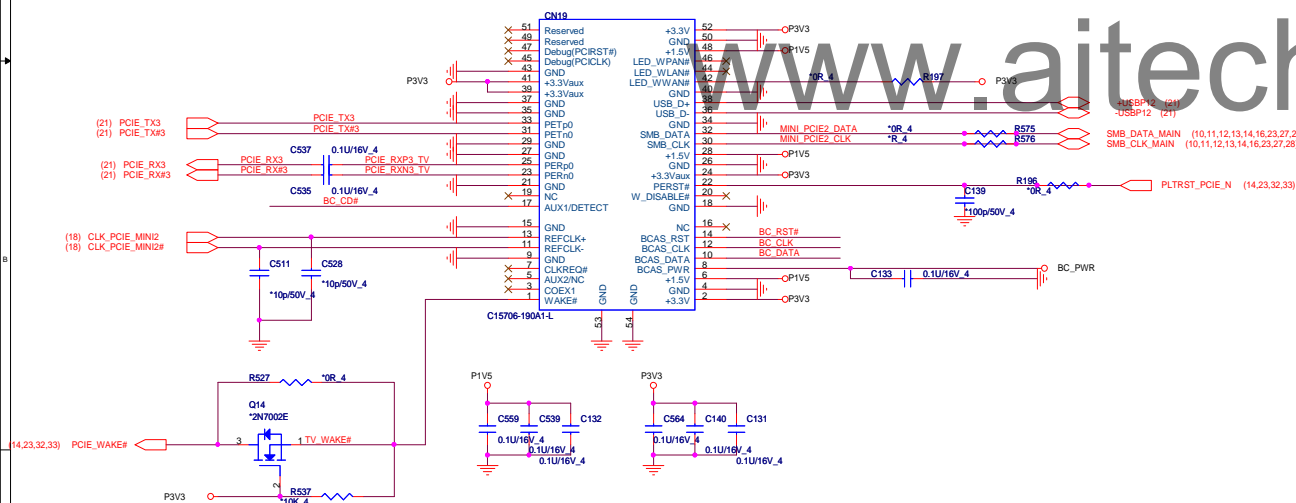
BT Connector

[ Activate: H ]

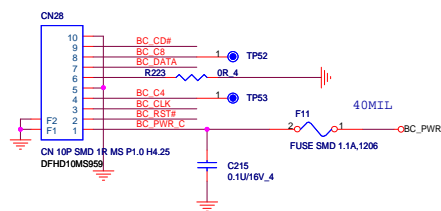
## Wireless / 80 Port



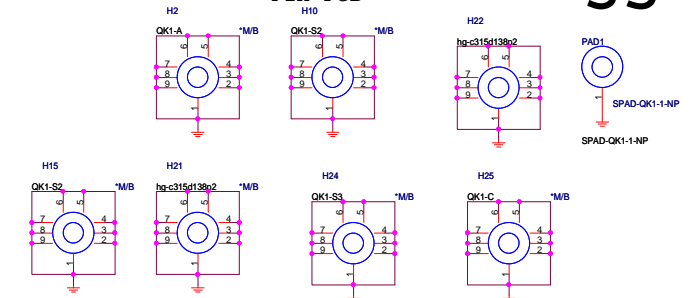
## TV Card



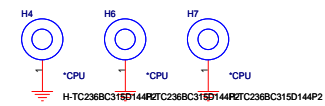
## B-CAS CONN



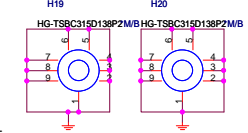
FIX PCB



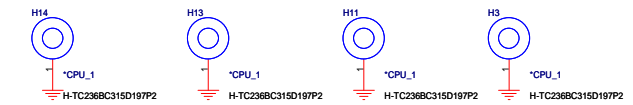
## CPU socket



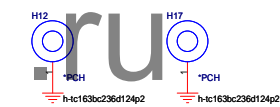
## I/O



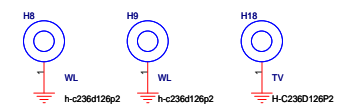
## CPU support



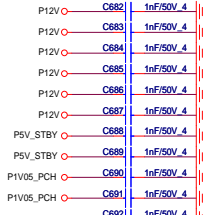
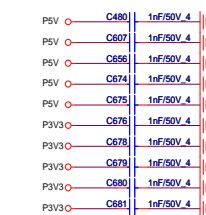
## PCH



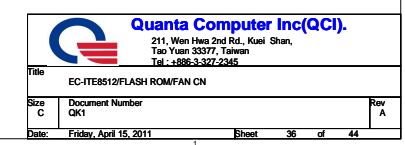
## WL/TV



FOR EMI

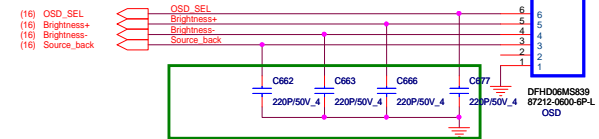
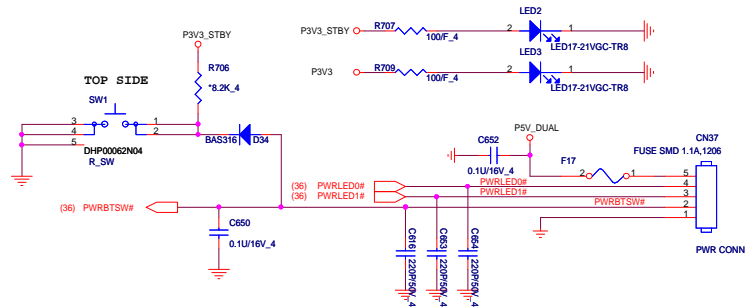


P1V1_VTT	C693	1nF/50V_4
P1V1_VTT	C694	1nF/50V_4
P1V1_VTT	C695	1nF/50V_4
VIN_CPU	C696	1nF/50V_4
VIN_CPU	C697	1nF/50V_4
V_AXG	C698	1nF/50V_4
V_AXG	C699	1nF/50V_4

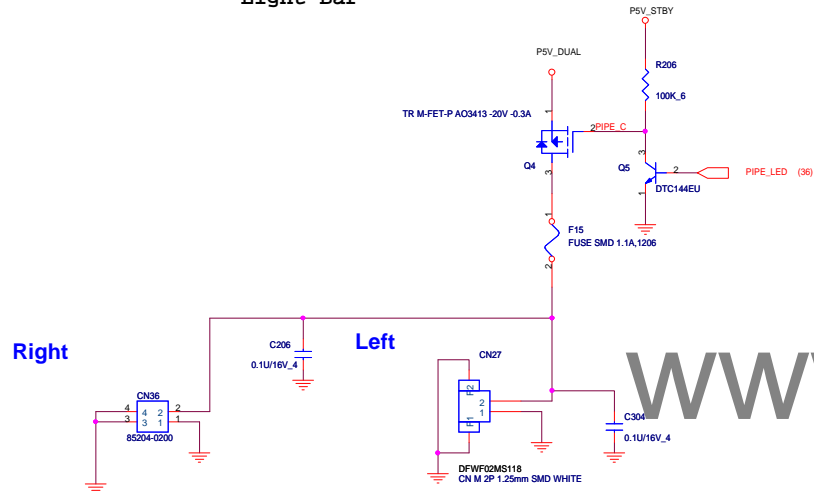




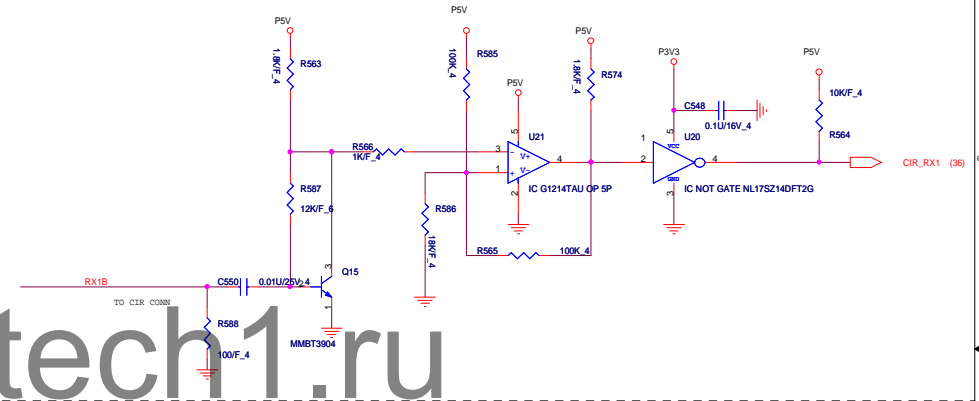
## POWER SW &amp; LED



## Light Bar

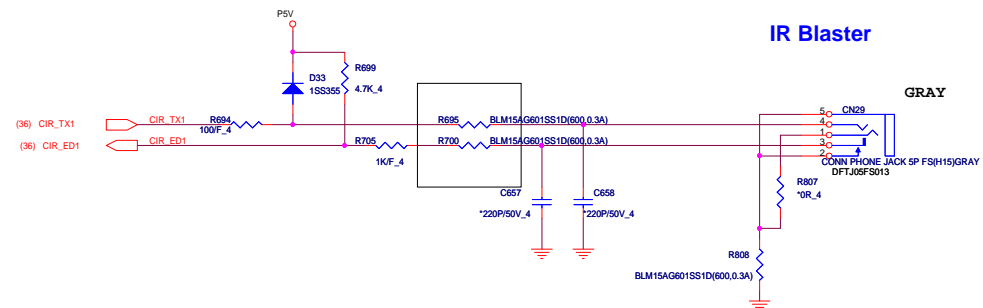


Add For EMI

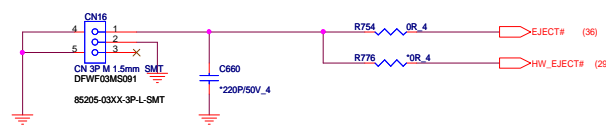


## IR Blaster

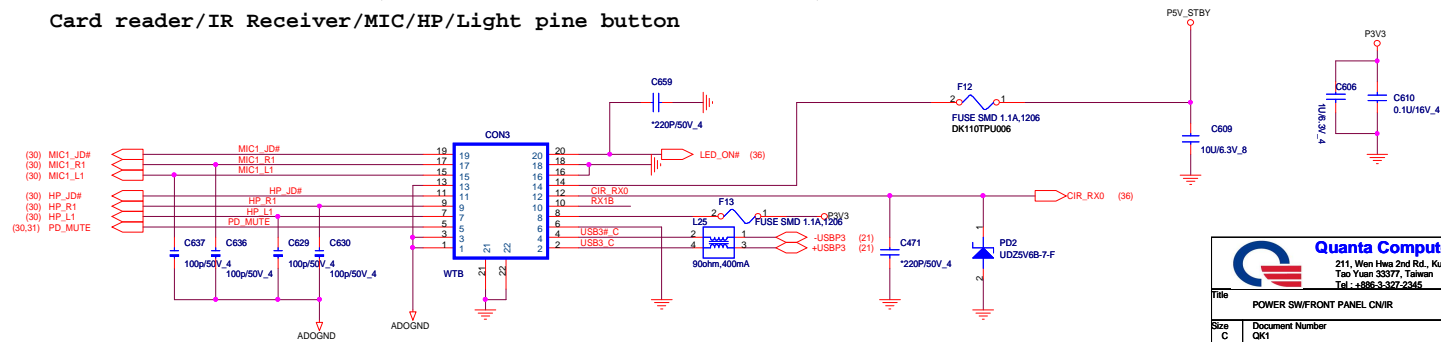
## IR Blaster

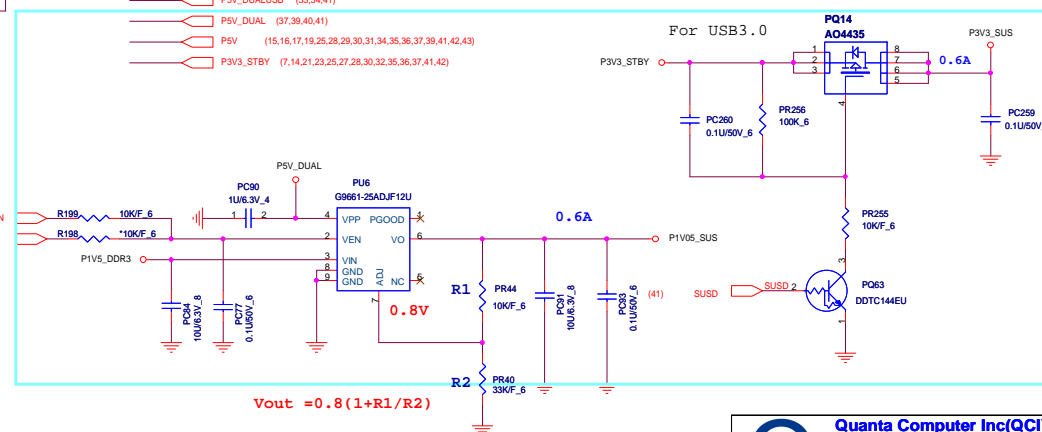
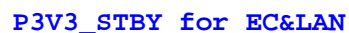
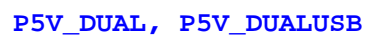


## ODD EJECT



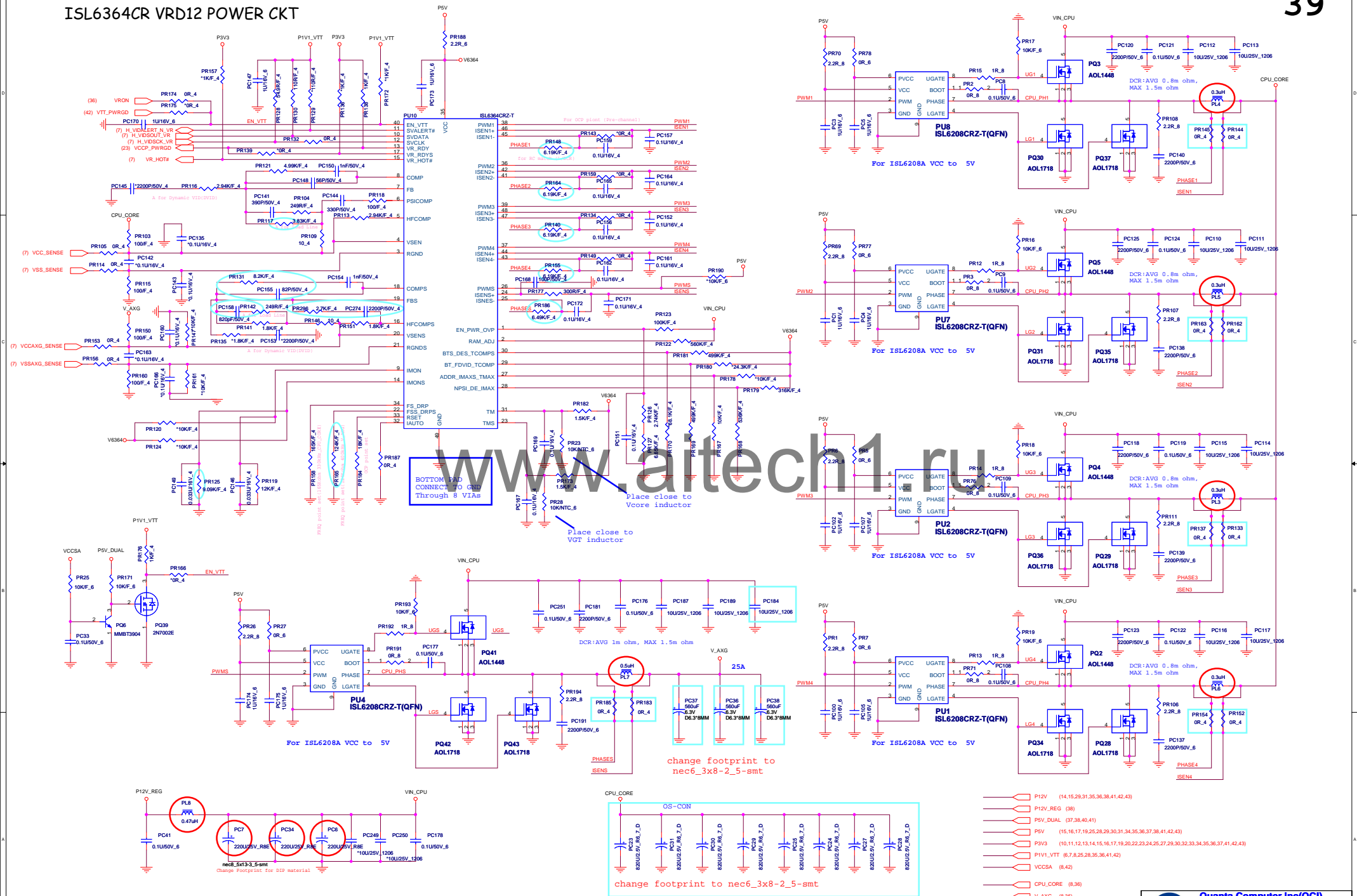
## Card reader/IR Receiver/MIC/HP/Light pine button

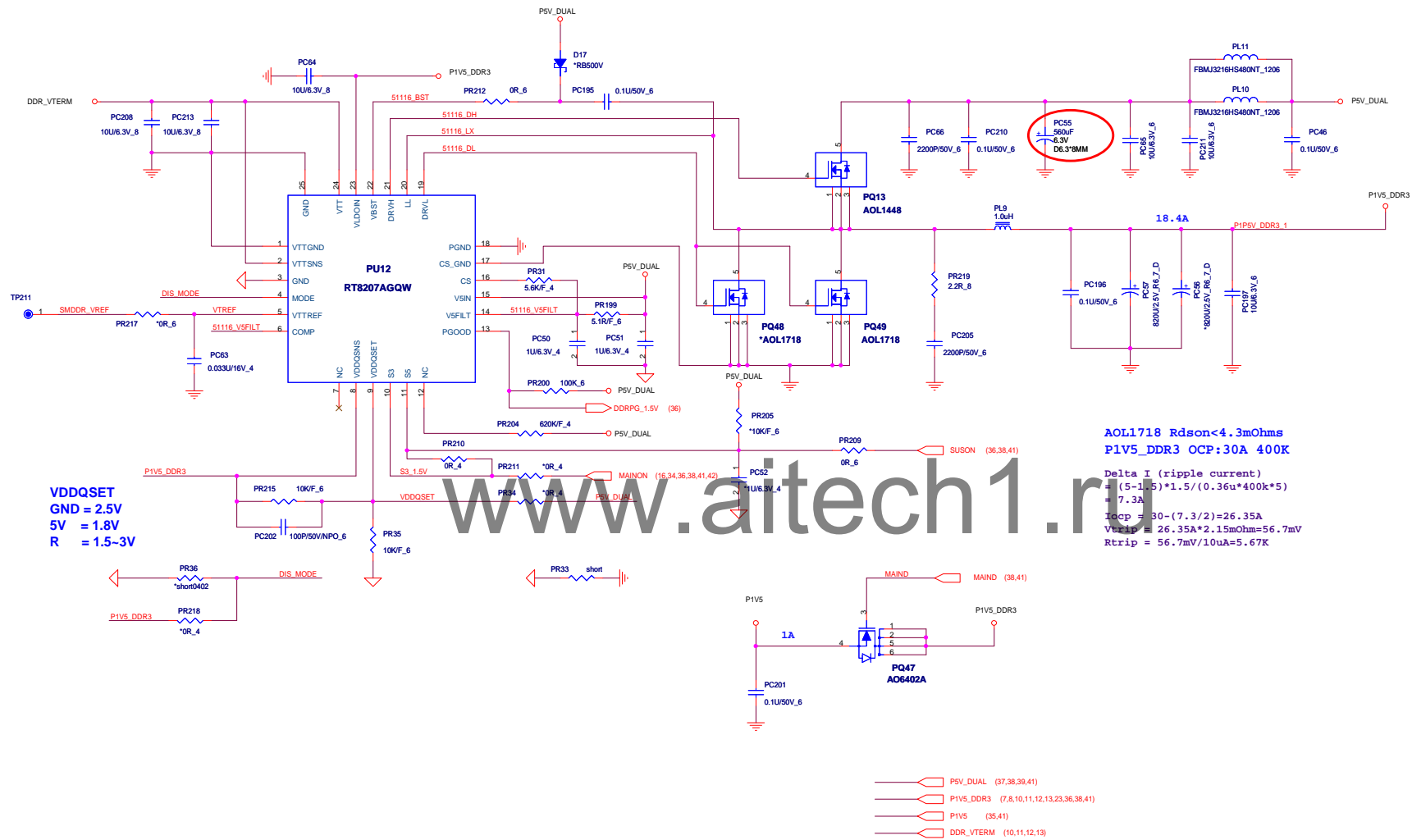


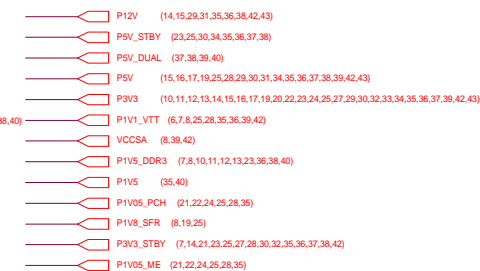
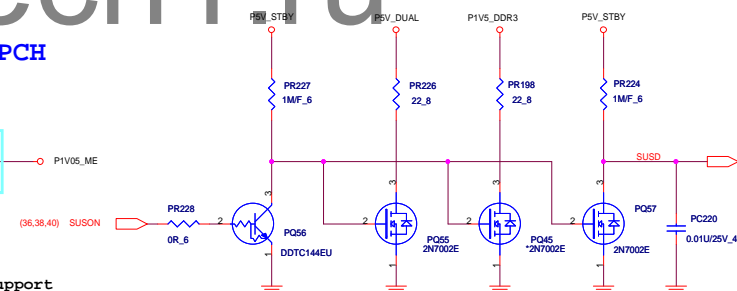
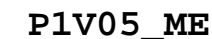


## ISL6364CR VRD12 POWER CKT

39

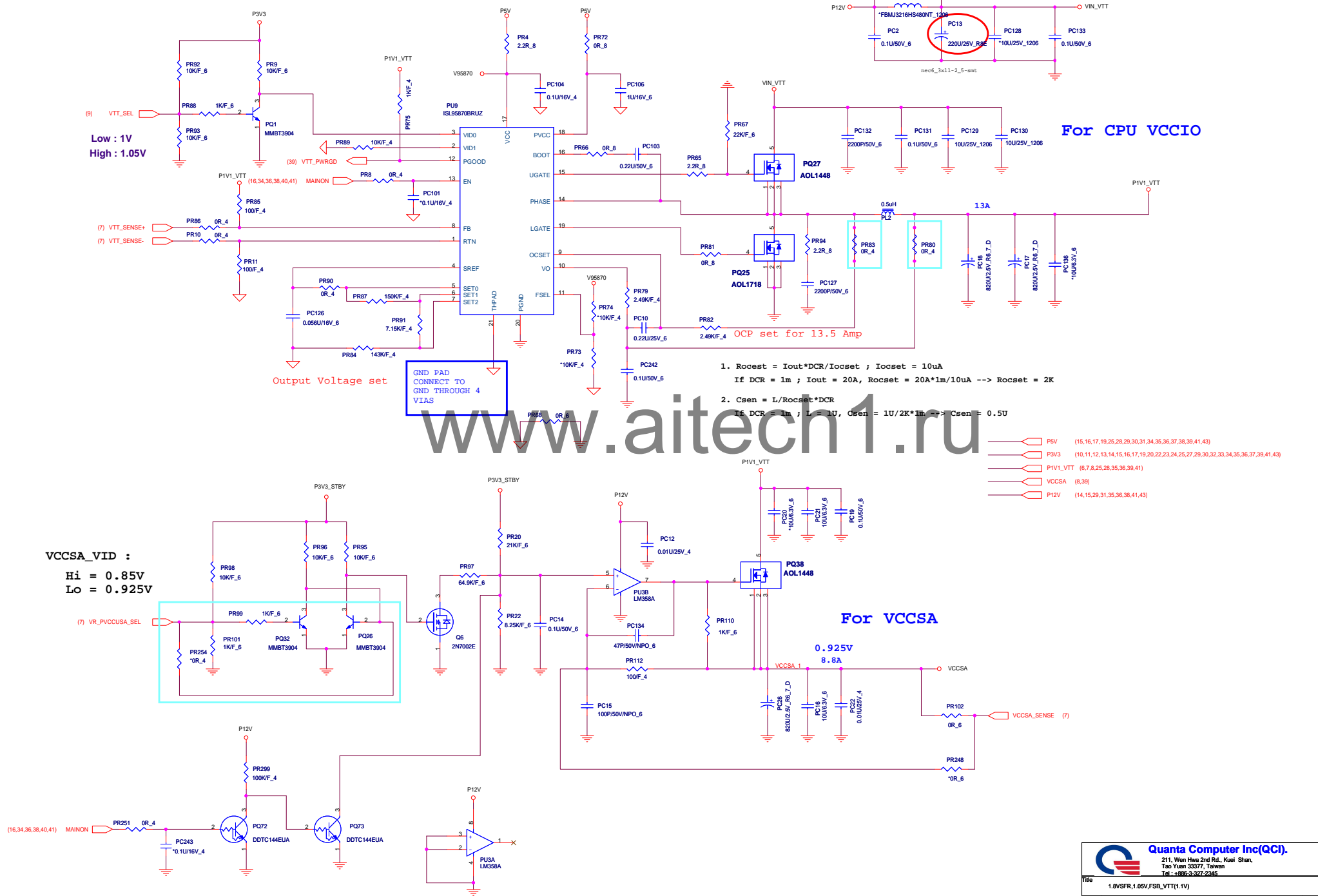




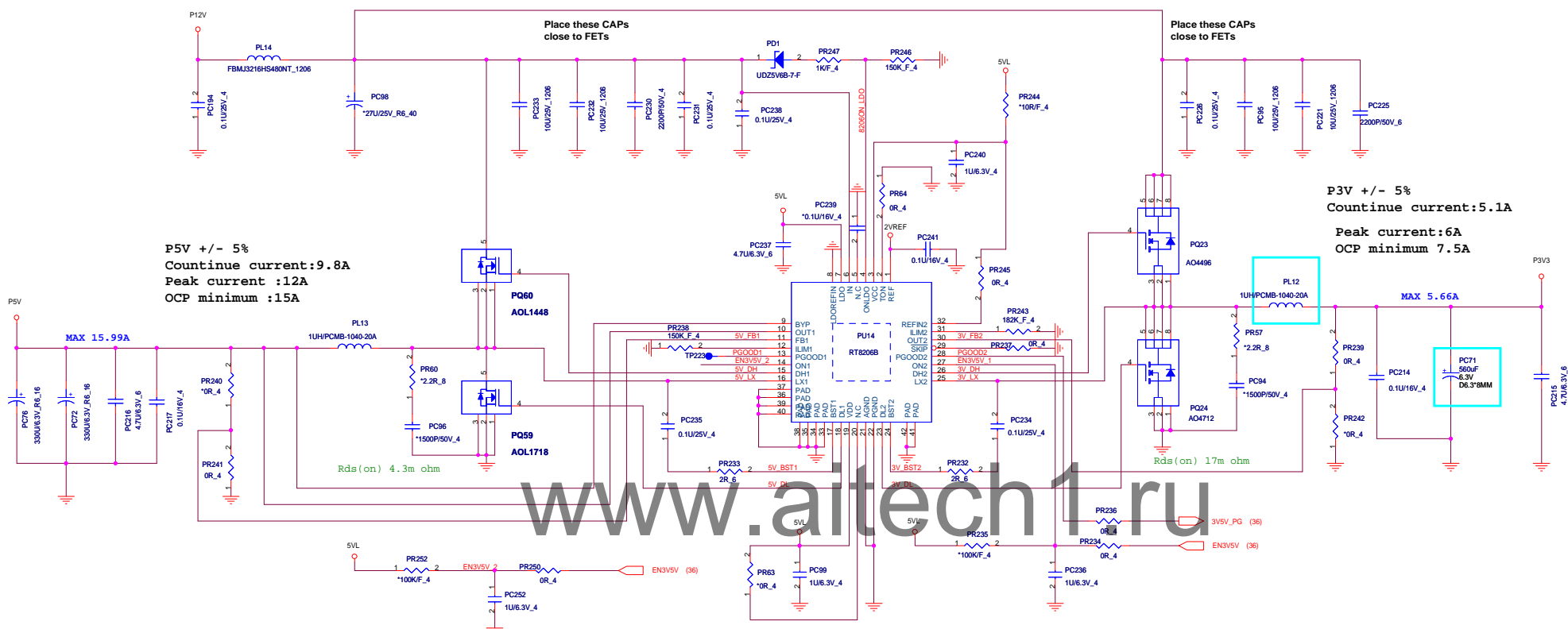


# ISL95870B For VTT

42



## SYSTEM POWER P3V3 / P5V



$$I_{ocp} = (V_{trip} / R_{ds\_on}) + (I_{ripple} / 2) = (V_{trip} / R_{ds\_on}) + (1 / (2 * L * f)) * (V_{in} - V_{out}) * V_{out} / V_{in}$$

AOL1718 MOSFET  $R_{ds\_on} = 3.4 \text{ m ohm} \sim 4.3 \text{ m ohm}$

5VPCU Operate Frequency by 400kHz

$R_{trip} = 150 \text{ K ohm}$

$V_{trip} = 150 \text{ K ohm} * 5/10 = 75 \text{ mV}$

$PL12 = 3.3 \text{ uH}$

$I_{ocp\_5VPCU} = 17.4 \sim 22 \text{ A}$

3VPCU Operate Frequency by 500kHz

$R_{trip} = 182 \text{ K ohm}$

$V_{trip} = 182 \text{ K ohm} * 5/10 = 91 \text{ mV}$

$PL8 = 4.7 \text{ uH}$   $I_{ocp\_3VPCU} = 6.06 \sim 5.05 \text{ A}$

P12V (14,15,29,31,35,36,38,41,42)  
 P5V (15,16,17,19,25,28,29,30,31,34,35,36,37,38,39,41,42)  
 P3V3 (10,11,12,13,14,15,16,17,19,20,22,23,24,25,27,29,30,32,33,34,35,36,37,39,41,42)



## PCB REV:B

2010/07/22:  
P31, Remove Buzzer circuit  
P15, Nexchange B\_EXP\_RX\_N1 and NB\_EXP\_RX\_P1  
2010/07/23:  
P39, PR225 change to 10K  
P35, Remove 3D RF circuit  
P38, ADD left pipe LED circuit, Change CN38 for Light and home button control  
P30, Remove CN11 SSD power CONN  
2010/07/27  
P24 ADD R714, ADD R713 Pull up H\_SKTOCC\_N  
P30. CN19 inverse 180 degree  
2010/07/28  
P4 Remove CLOCK GEN circuit  
P42 Remove PU6, PR51  
P24 DEL Q4,Q5  
P28 Remove Q7

## PCB REV:D

2010/10/21:  
P19, Add Q34,Q35,R732,R733,R752,R753 for DP ctrl level shift  
P34, Add U34,C209,C211,R758,R759 for usb charge  
2010/11/03:  
P37,CON5 modify pin define.  
2010/11/04  
P37,CN27,CN36 Pin1,2 exchange  
2010/11/05:  
P37,Add R754,R776,R777 for odd eject  
P34,Add CN42 for touch power  
2010/11/17:  
P16,Add CN21 for DVI EDID Flash  
P33,Add R778,R779,R780,R787 for USB 3.0  
P37,Del R216,R708,C648,Q26  
2010/11/22  
1.P15 CN1 change CONN for EMI issue  
2010/11/23  
1.DelR247,R248,R674,R655,R710,R712,R697,R698,R692,R693 for EMI  
2.Add RN1~RN7 for EMI  
3.P16,Del con2,add CN43 for EMI  
2010/11/24  
1.P30,Add Q36,D28 for AUDIO  
2.P31,Add Q26,Q31 for Audio mute  
2010/11/26  
1.Add PD2 for CIR  
2.Add R247、R248、R405、R654、R672、R674、R687、R688、R693、R697、R698、R703 for EMI

## Power portion

1. Page 31. Audio Power source PVDD output circuit
2. Page 38. Change PSU connector to 6pin and 10 pin, add component location PC53, PC249 for 5VSTBY source
3. Page 40. Change PU12 pin17 connect line to GND, change location PL9 footprint
4. Page 40. Change PU12 pin17 connect line to GND, change location PL9 footprint

## PCB REV:E

1. Page 30. Q36 change type from 2n7002 to DTC144EU for audio
- 2010/12/16
1. Page 28. Add R351,R711,R712
- 2010/12/28
1. Page 30. Add BZ1 (reserve Buzzer)

2011/01/24

1. Page 15. Del R234,R239 Add F7,F8 for safety
2. Page 34. Del R177, Add F9,F10,F16 for safety
3. Page 35. Add F11 for safety
4. Page 37. Del R638,R216, Add F12,F13,F15,F17 for safety
5. Page 34. Add C297,C302 for EMI

## PCB REV:F

1. Page 17. Del D31,D43 add R801,R802 for HDMI Sink
2. Page 23. C108, C109 change to 15pF
3. Page 38. PQ14 change type from SI4116DY to AO4435 for USB30
4. Page 38. Remove R628、R634、add L25 for EMI

Change List			
Title		Rev	
Size	Document Number	<Rev Code>	
C	QK1		
Date:	Friday, April 29, 2011	Sheet	44 of 44